LCFC Confidential

ADL-P LCFC P/S Schematics Document

Phoenix / Serval-2 M/B SCHEMATICS

Intel Alder Lake Processy with LPDDR5

REV:1.0

Title	<Title>		
Size	Document Number		Rev
Custom	T14s Gen2		0.1
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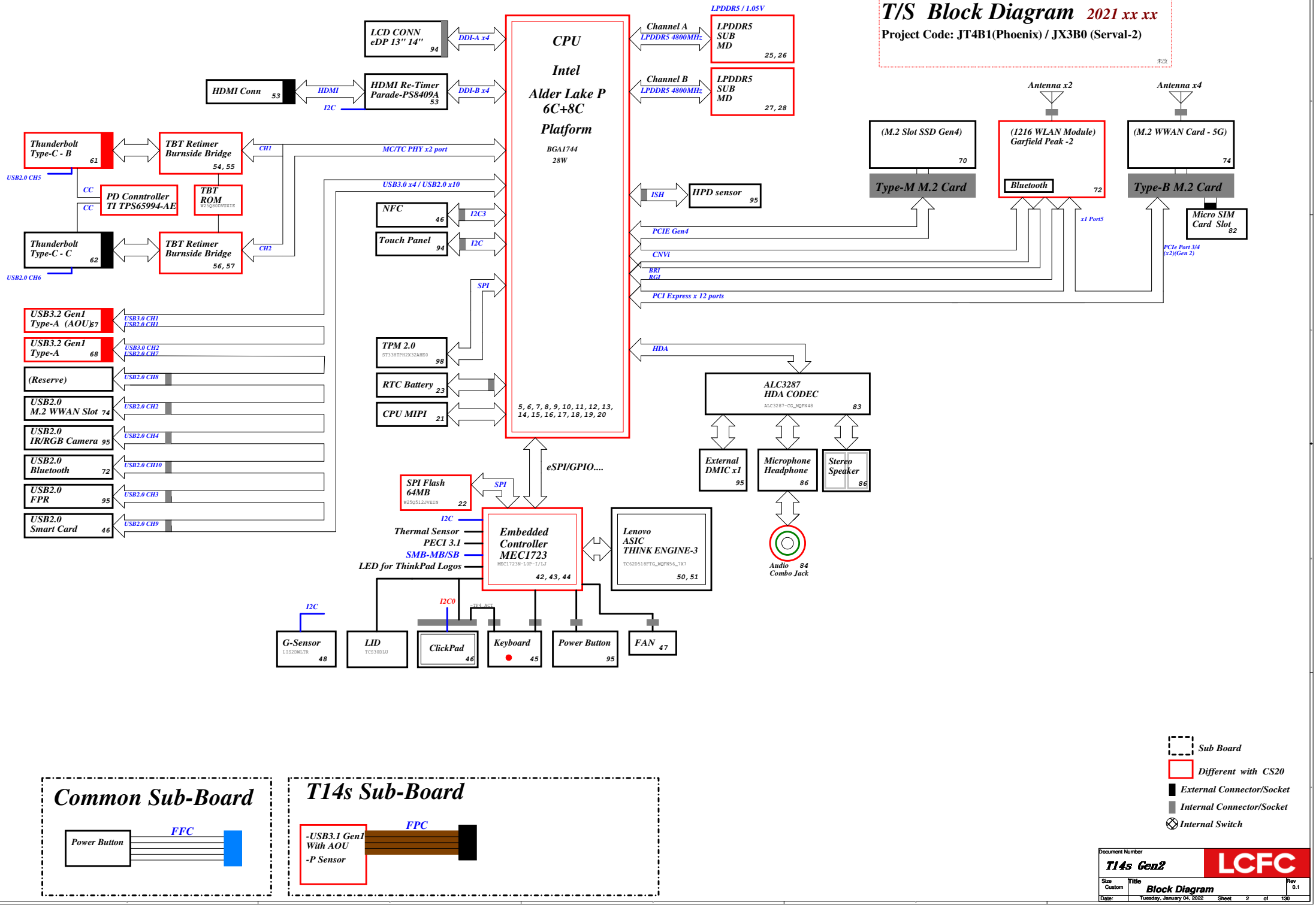
T/S Block Diagram 2021 xx xx

Project Code: JT4B1(Phoenix) / JX3B0 (Serval-2)



Common Sub-Board

T14s Sub-Board

Sub Board

Different with CS20

External Connector/Socket

Internal Connector/Socket

Internal Switch

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LPDDR5_BOM_CONFIG

X76	DRAM Option	MEMORY Configure Option
Hynix 8G	H9JCNNNBK3MLYR-N6E	MEMORYID4 MEMORYID3 MEMORYID2 MEMORYID1 MEMORYID0
Micron 8G	MT62F512M32D2DR-031	
Hynix 16G	H9JCNNNCP3MLYR-N6E	
Micron 16G	MT62F1G32D4DR-031	
Samsung 16G	K3LKBKB0BM-MGCP	
Hynix 32G	H9JCNNNFA5MLYR-N6E	
Micron 32G	MT62F2G32D8DR-031	
Samsung 32G	K3LKCKC0BM-MGCP	

MP_CPU_BOM_CONFIG_U28

ADL-U28 4+8 Non Vpro
- NV_i5-1240P SA0000D0Q10 D0Q@
- NV_i7-1260P SA0000D0P10 D0P@

ADL-U28 4+8 Vpro
- V_i5-1250P SA0000D1100 D11@
- V_i7-1270P SA0000D1000 D10@

ADL-U28 6+8 Vpro
- V_i7-1280P SA0000CY310 CY3@

MP_WLAN_BOM_CONFIG

Garfield Peak2 vPro
- Garfield Peak2 AX211.D2WG_999M5N PK29S001T10 GP2_MP@

MP_PCB_BOM_CONFIG

PCB
- PCB JX3B0 NM-E091 NS-E091/NS-E092 V1/V1/V1 DA20A800100 SVT@

MB
- PCB JX3B0 NM-E091 REV1.0 M/B DA80007S10 MB@

PWR
- PCB JX3B0 NS-E091 REV1.0 PWR W/ FPR/B DA80007T10 PWR@

USB
- PCB JX3B0 NS-E092 REV1.0 USB/B DA80007U10 USB@

SITR_CPU_BOM_CONFIG NOT MP,MP CPU NOT RELEASED,NEED TO MODIFY

ADL-U15 2+8 Non Vpro
- NV_i5-1235U SA0000D1S10 D1S@
- NV_i5-1235U_no-IPU SA0000D2P00 D2P@

ADL-U15 2+8 Vpro
- V_i5-1245U SA0000D1T10 D1T@

ADL-U15 2+4 Non Vpro
- NV_i3-1215U SA0000D2S00 D2S@

MP_CPU_BOM_CONFIG_U15

ADL-U15 2+8 Non Vpro
- NV_i5-1235U SA0000D1S40 D1S40@

ADL-U15 2+8 Vpro
- V_i5-1245U SA0000D1T30 D1T30@

ADL-U15 2+4 Non Vpro
- NV_i3-1215U SA0000D2S30 D2S30@

PCB_BOM_CONFIG

PCB
- PCB 2DA NM-E091 REV0 M/B DA80007S00 SIT@

WLAN_BOM_CONFIG

Garfield Peak2 vPro
- Garfield Peak2 AX211.D2WG GP2@

Qualcomm WLAN
- Qualcomm NFA-725A PK29S001X00 Qual@

TPM_BOM_CONFIG

TPM
- ST SA0000C8600 ST@
- Nuvoton SA0000C3000 NUVOTON@
- NationZ SA0000C1S00 NationZ@
- Infineon SA0000C3310 Infineon_72@

TPM_BOM_CONFIG_OLD

TPM_OLD
- ST SA0000AB720 ST_OLD@
- Nuvoton SA00008KS30 NUVOTON_OLD@

QS CPU_BOM_CONFIG

ADL-U28 4+8 Non Vpro
- NV_i5-1240P SA000C5R00 U28_4+8_CSR@
- NV_i7-1260P SA000C5K00 U28_4+8_CSK@

ADL-U28 4+8 Vpro
- V_i5-1250P SA000C5S00 U28_4+8_CSS@
- V_i7-1270P SA000C5P00 U28_4+8_CSP@

ADL-U28 6+8 Vpro
- V_i7-1280P SA000C5J00 U28_6+8_CSJ@

SIT2 Supp_QS CPU_BOM_CONFIG

ADL-U28 4+8 Non Vpro
- NV_i7-1260P SA000CY500 U28_4+8_CY5@
- NV_i5-1240P SA000CY700 U28_4+8_CY7@

ADL-U28 4+8 Vpro
- V_i7-1270P SA000CY600 U28_4+8_CY6@
- V_i5-1250P SA000D1110 U28_4+8_D11@

ADL-U28 6+8 Vpro
- V_i7-1280P SA000CY300 U28_6+8_CY3@

427201_ADL P_PDG_Rev1.0

Rails	S4 Vr	S4/ Rail	CS0	S0ix/ Rail	S3/ S4	S3/ Rail	S4 /S5 (CS) Rail	S4 /S5 (CS) Rail	Deep S4 / S5	pseudoG3	True G3
VCCCORE	A0	ON	ON[1]	OFF	OFF	OFF	OFF	OFF	OFF	No Power	No Power
VCCST	A0	ON	ON[1]	OFF	OFF	OFF	OFF	OFF	OFF	No Power	No Power

Notes:
1. The state of the system without RTC well powered can also be considered True G3. In Pseudo G3, only RTC rail is powered off.
2. S0_PG_PHY rails may turn off if the VIDs are low.
3. S0/M2 state includes all Package C-states from C0-C10
4. Assume SLP_S0# and CPU_C10_GATE# have asserted from the PCH
5. S4/S5 and X1.8M are platform rails used to supply external devices when ME operates during S4/M3 states. These rails are not used directly by the CPU, and are not present on non-M3 supported systems
6. NA
7. NA
8. NA
9. NA
10. Rail as M3 support on external devices, V3.3M/V1.8M will be OFF in S4/M3
11. NA
12. If VCCIN_AUX is ON, VCCIPS_PROC needs to be ON
13. VCCIPS_PROC can be turned ON in S5 state through VCCIP_OVERRIDE
14. VCCIPS_PROC can be turned OFF in S0 state through VCCIP_OVERRIDE
15. For systems that use PSYS based PCH parts the processor requires that any time AUX is ON at a non-zero voltage, VCCIPS_PROC must be ON at a non-zero voltage. For PSYS based PCH parts that use the AUX VIDs as part of the scalable logic since AUX can be ON in S0 states with PSYS based PCH parts.
16. NA
17. This supply is expected to be OFF during states where CPU_C10_GATE# is asserted. If rails do not go during this condition but the processor will not achieve it's lowest power consumption. Specific power up sequence requirements may apply.
18. If MIPI is not used, VCC_DISPIO power rail will be powered by VCCIPS_PROC_OUT and always ON in S0ix. If MIPI is used with a LDO to make 1.24V its enable should be controlled by CPU_C10_GATE# to allow shutdown.
19. VCC_RDP1LP must ramp with or after VCCIPS_PROC_OUT. Recommend before DNXP for ease of implementation. While exiting from S0ix, must be ramped within 60us. No specific order required for discharge recommended.

10.10.4 Power States

Table 732. System with M3 State Supported

Rails	S4 Vr	S0/ Rail	CS0[1]	S0ix/ Rail	S3/S4	S3/ Rail	S4 /S5 (CS) Rail	S4 /S5 (CS) Rail	Deep S4 / S5	pseudoG3[2]	True G3[3]
VCCRTC	A0	ON	ON	ON	ON	ON	ON	ON	ON	No Power	No Power
VCCDSW_3P3	A0	ON	ON	ON	ON	ON	ON	ON	No Power	No Power	No Power
VBATA (VDC)	A0	ON	ON	ON	ON	ON	ON	ON	No Power	No Power	No Power
VCCPRIM_3P3	A0	ON	ON	ON	ON	ON	ON	OFF	No Power	No Power	No Power
VCCPRIM_1P8	A0	ON	ON	ON	ON	ON	ON	OFF	No Power	No Power	No Power
VCC_VNNRET_LPSS	P	ON	ON	ON	ON	ON	ON	OFF	No Power	No Power	No Power
VCC_V1P05SET_LPSS	P	ON	ON	ON	ON	ON	ON	OFF	No Power	No Power	No Power
V3.3MT	A0	ON	ON	OFF	ON[17]	OFF	ON[17]	OFF	No Power	No Power	No Power
V1.8MT	A0	ON	ON	OFF	ON[17]	OFF	ON[17]	OFF	No Power	No Power	No Power
VDD2	A0	ON	ON	ON	ON	OFF	OFF	OFF	No Power	No Power	No Power
VPP	A0	ON	ON	ON	ON	OFF	OFF	OFF	No Power	No Power	No Power
VCCIP01_PROC	A0	ON	ON	ON/OFF[11]	ON/OFF[11]	ON/OFF[11]	ON/OFF[11]	OFF	No Power	No Power	No Power
VCCIN_AUX	A0	ON	ON[14]/OFF[15]	ON[14]/OFF	ON[14]/OFF	ON[14]/OFF	ON[14]/OFF	OFF	No Power	No Power	No Power
VCCIP8_PROC	P	ON	ON[14]/OFF[15]	ON[14]/OFF	ON[14]/P.U.P.D	ON[14]/P.U.P.D	ON[14]/OFF	OFF	No Power	No Power	No Power
VCC_RDP1LP[19]	P	ON	OFF[18]	OFF[18]	OFF	OFF	OFF	OFF	No Power	No Power	No Power

continued...

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T/S SIT-R Planar Logic Schematics

T/S
VER 0.5
Dec/09/2021

BASE LOGIC : T14s GEN3_SIT_0909_V0.3_BOM

1.Project Name
2.BLOCK DIAGRAM
3.EC list
4.TITLE PAGE
5.CPU(1/16) : DDI/EDP
6.CPU(2/16) : DDR (1/2)
7.CPU(3/16) : DDR (2/2)
8.CPU(4/16) : MISC/JTAG
9.CPU(5/16) : LPC/SPI/SMBUS/C-LINK
10.CPU(6/16) : LPSS/ISH
11.CPU(7/16) : AUDIO
12.CPU(8/16) : PCIE/USB/SATA
13.CPU(9/16) : CSI-2/EMMC/CNVI
14.CPU(10/16) : CLOCK SIGNALS
15.CPU(11/16) : SYSTEM PM
16.CPU(12/16) : CPU POWER (1/2)
17.CPU(13/16) : CPU POWER (2/2)
18.CPU(14/16) : PCH POWER
19.CPU(15/16) : GND
20.CPU(16/16) : CFG/RESERVED
21.MIPI60 DEBUG PORT
22.SPI FLASH
23.RTC
24.BLANK
25.LPDDR5 CHANNEL 0&1
26.LPDDR5 CHANNEL 2&3
27.LPDDR5 CHANNEL 4&5
28.LPDDR5 CHANNEL 6&7
29.BLANK
30.BLANK
31.BLANK
32.BLANK
33.BLANK
34.BLANK
35.BLANK
36.BLANK
37.BLANK
38.BLANK
39.BLANK
40.BLANK
41.BLANK
42.MEC1503 (1/3)
43.MEC1503 (2/3)
44.MEC1503 (3/3)
45.KEYBOARD/TRACK POINT
46.TOUCH PAD/Smart card/NFC
47.FAN CONNECTOR
48.APS G-SENSOR
49.BLANK
50.THINK ENGINE-3 (1/2)
51.THINK ENGINE-3 (2/2)
52.BLANK
53.HDMI CONNECTOR
54.THUNDERBOLT RETIMER B (1/2)
55.THUNDERBOLT RETIMER B (2/2)
56.THUNDERBOLT RETIMER C (1/2)
57.THUNDERBOLT RETIMER C (2/2)
58.BLANK
59.USB PD CONTROLLER
60.BLANK
61.TYPE-C with THUNDERBOLT C
62.TYPE-C with THUNDERBOLT B
63.BLANK
64.BLANK
65.TYPEC_DCIN
66.BLANK
67.USB TYPE-A CONNECTOR
68.USB TYPE-A CONN
69.BLANK
70.M.2 SOCKET 3 MODULE I/F
71.BLANK
72.M.2 TYPE 1216 MODULE
73.BLANK
74.M.2 SOCKET 2 MODULE I/F
75.BLANK
76.BLANK
77.BLANK
78.BLANK
79.BLANK
80.BLANK
81.BLANK
82.BLANK
83.AUDIO CONNECTOR
84.AUDIO SMART AMP
85.AUDIO SPEAKER
86.AUDIO BEEP
87.BLANK
88.BLANK
89.BLANK
90.BLANK
91.BLANK
92.BLANK
93.SMART CARD READER
94.LCD & TOUCH PANEL INTERFACE
95.LID/CAMERA/MIC/SENSOR INTERFACE
96.BLANK
97.BLANK
98.DISCRETE TPM 2.0
99.BLANK
100.DC-INPUT
101.BATTERY INPUT
102.BATTERY CHARGER
103.DC/DC VCC5M
104.BLANK
105.DC/DC VCC3M
106DC/DC VCC1R2A/2R5A
107.DC/DC VCC5M_PD
108.DC/DC VCCCPUCORE (MP2940A)
109.DC/DC VCCCPUCORE (MP86941*2)
110.DC/DC VCCCPUCORE (MP86941*1)
111.DC/DC VCCPCHCORE(MP2941B)
112.BLANK
113.BLANK
114.DC/DC VCC1R8_SUS
115.BLANK
116.BLANK
117.BLANK
118.BLANK
119.BLANK
120.LOAD SW VCC3_SUS
121.LOAD SW LAN
122.LOAD SW B
123.LOAD SW TOUCH PANEL & SSD
124.BLANK
125.BLANK

Lenovo

Project Name : T14s Gen2	Title : TITLE PAGE
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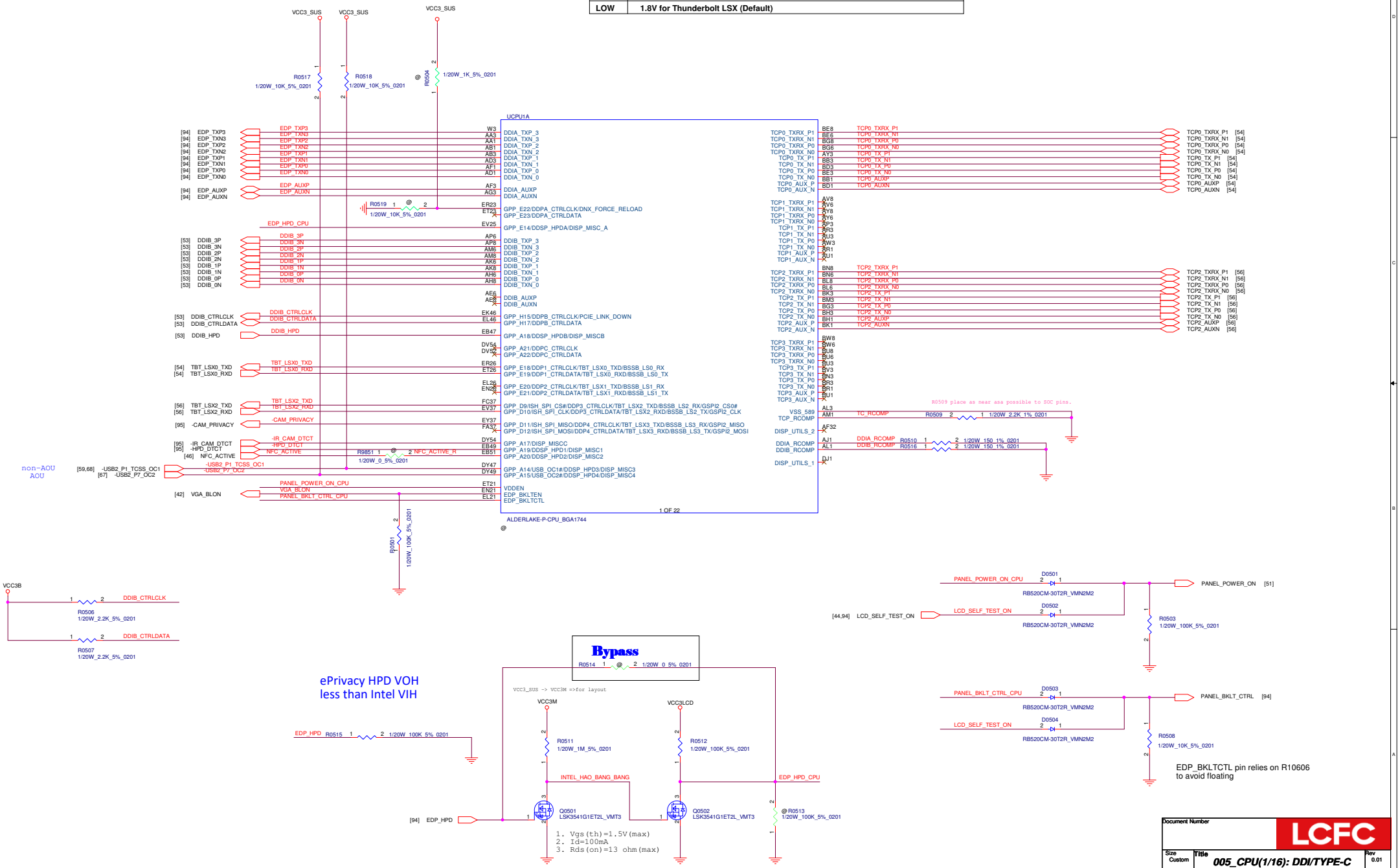
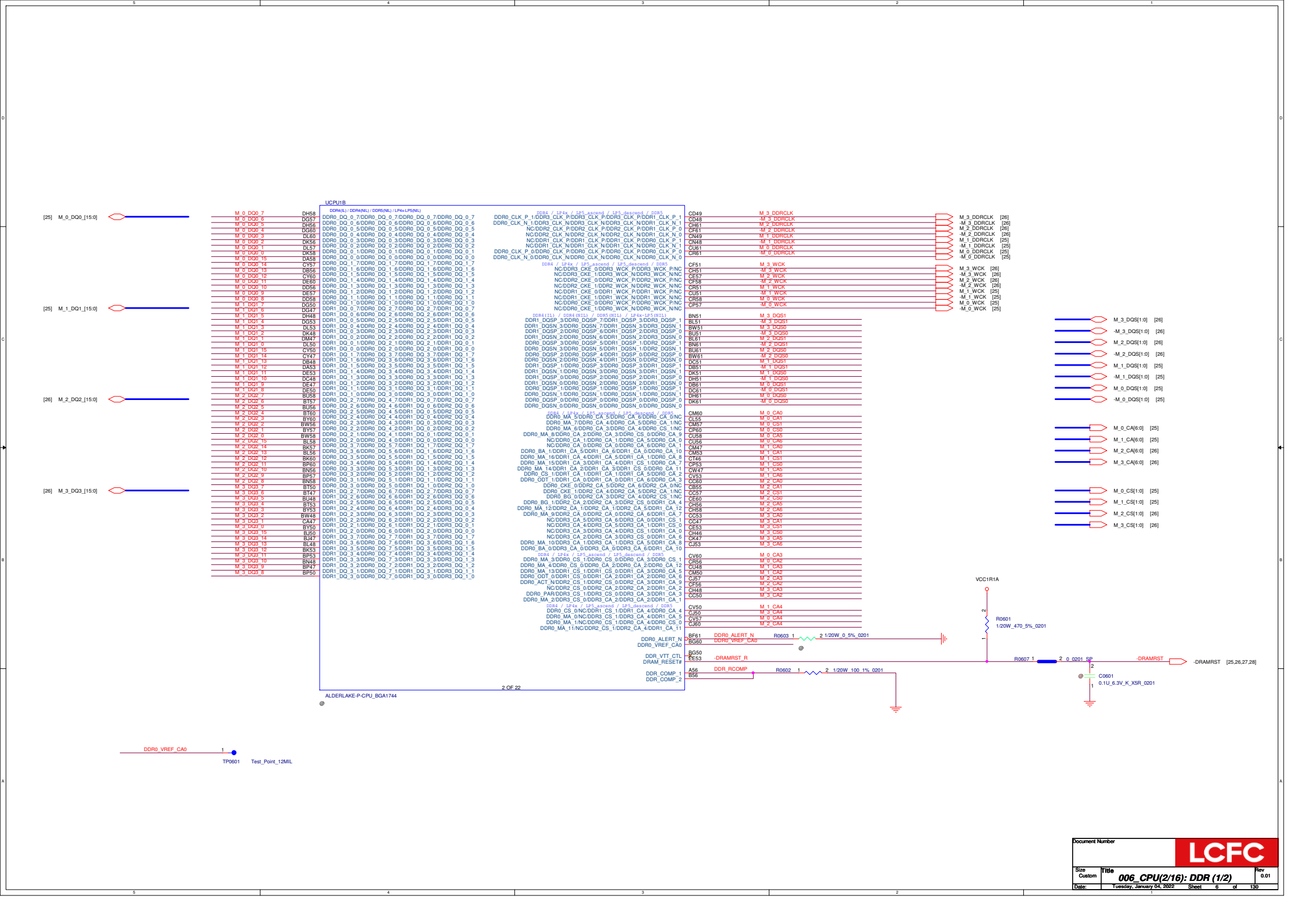
TABLE : Functional Strap

GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD (DDP1 I2C / TBT_LSX0 Pin VCC Configuration)	
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD (DDP2 I2C / TBT_LSX1 Pin VCC Configuration)	
GPP_D10/DDP3_CTRLDATA/TBT_LSX2_RXD (DDP3 I2C / TBT_LSX2 Pin VCC Configuration)	
GPP_D12/DDP4_CTRLDATA/TBT_LSX3_RXD (DDP4 I2C / TBT_LSX3 Pin VCC Configuration)	
HIGH	**3.3V for HDMI Display I2C (External Pull-Up Resistor Required)**
LOW	**1.8V for Thunderbolt LSX (Default)**





Document Number	LCFC
Size: Custom	Title: 006_CPU(2/16): DDR (1/2)
Rev: 0.01	
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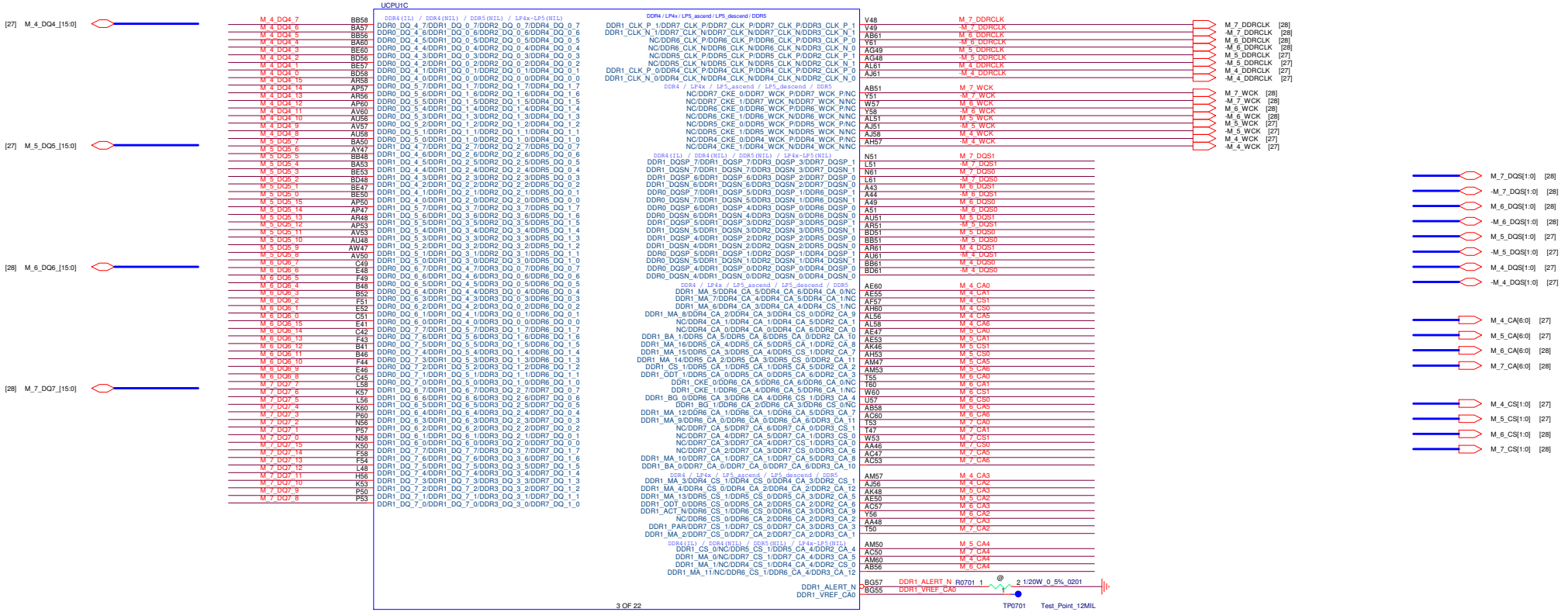

Document Number			LCFC
Size: Custom	Title: 007_CPU(3/16): DDR (2/2)		Rev: 0.01
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Figure 153. CPU Sideband - PROCHOT Topology

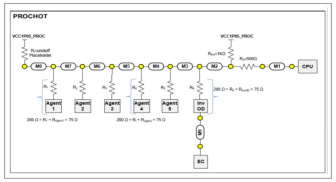
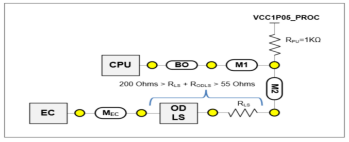


Figure 157. CPU Sideband - THERMTRIP



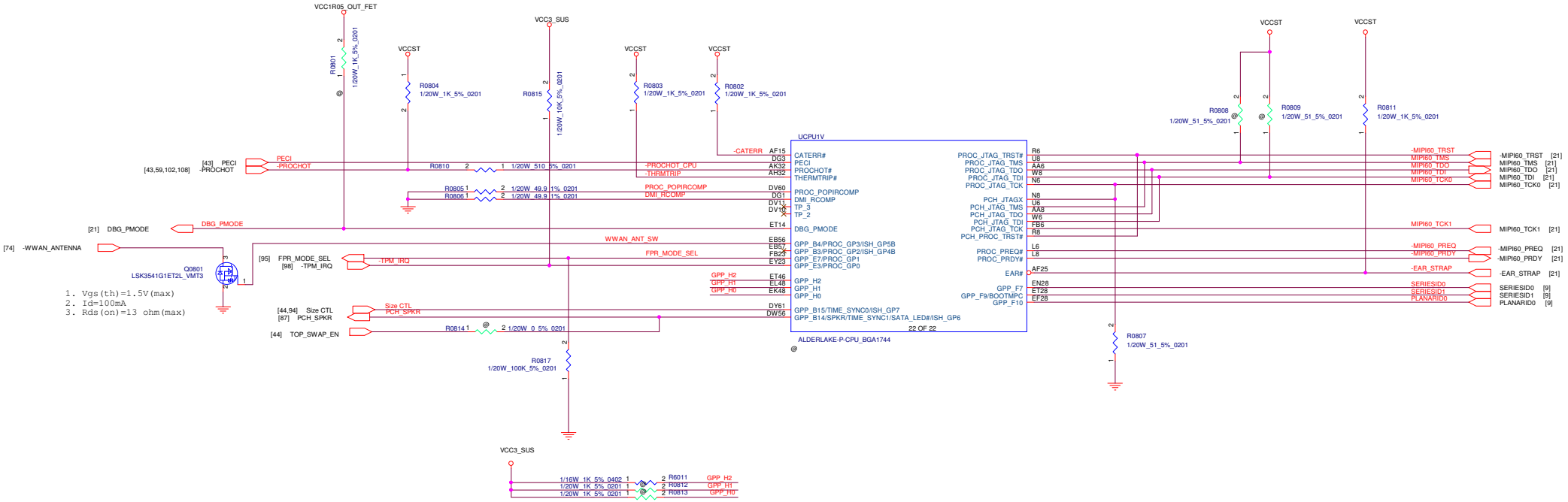


TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default)

← LOGIC

TABLE : Functional Strap

DBG_PMODE (DFx Test Mode)	
HIGH	DFx Test Mode Disabled (default)
LOW	DFx Test Mode Enabled

TABLE : Functional Strap

GPP_F7 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

TABLE : Functional Strap

GPP_F10 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

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Document Number			LCFC
Size: Custom	Title: 008_CPU(4/16): Misc/JTAG		Rev: 0.01
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TABLE : Functional Strap

SPI0_MOSI (Boot Halt)	
HIGH	Disabled
LOW	Enabled

← LOGIC

TABLE : Functional Strap

SPI0_IO2 (Consent Strap)	
HIGH	Disabled
LOW	Enabled

← LOGIC

TABLE : Functional Strap

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled
LOW	Enabled

← LOGIC

TABLE : Functional Strap

GPP_E6 (JTAG ODT Disable)	
HIGH	JTAG ODT Enabled
LOW	JTAG ODT Disabled

← LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

TABLE : Functional Strap

GPP_B23/SML1ALERT#/PCHHOT# (CPUNSSC Clock Frequency)	
HIGH	19.2MHz Clock (Derived from 38.4MHz Crystal)
LOW	38.4MHz Clock (Direct from Crystal) (Default)

← LOGIC

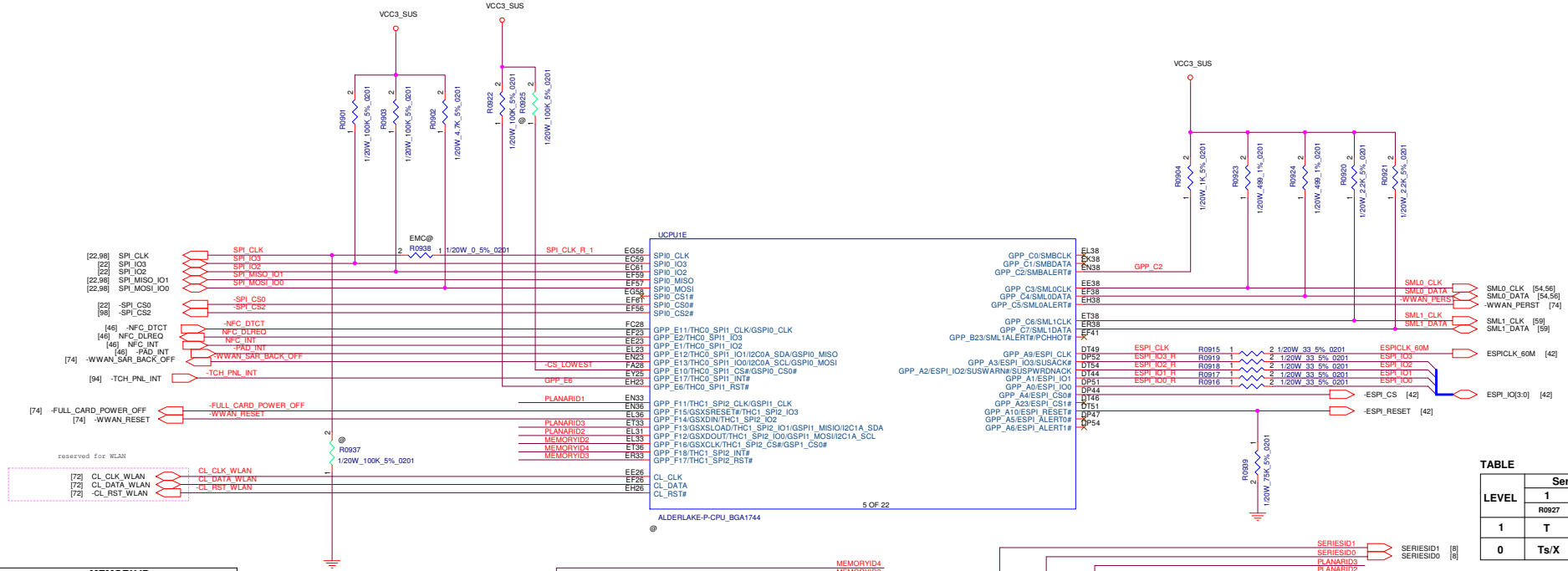
TABLE : Functional Strap

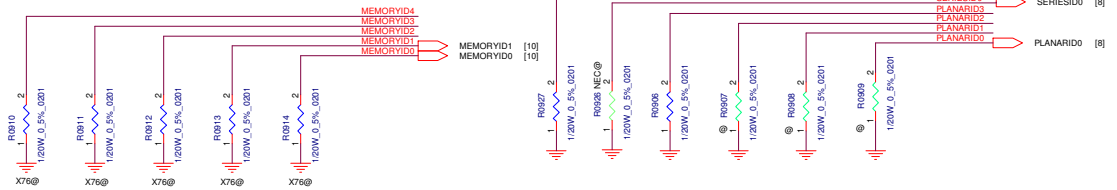
GPP_C5/SML0ALERT# (Boot Strap Bit 0)	
GPP_H0 (Boot Strap Bit 1)	
GPP_H1 (Boot Strap Bit 2)	
GPP_H2 (Boot Strap Bit 3)	
0000b	Master Attached Flash Configuration eSPI is enabled
0010b	Master Attached Flash Configuration eSPI is disable
0100b	BIOS on eSPI Peripheral Channel CSME on master attached device
1000b	Slave Attached Flash Configuration
1100b	BIOS on eSPI Peripheral Channel CSME on slave attached SPI

← LOGIC

Project	Phoenix/Serval2		Remark
PD Controller	TPS65994AE		
Topology	PD Port A	PD Port B	
	TCP2	TCP0	
	TBT4	TBT4	
netname	TBTC	TBTB	
I2C1 SCL/SDA netname	I2C1_CLK_PD	I2C1_DATA_PD	
To where	EC		
Address	0x20	0x24	Set in PD FW,ME Fit Set in PD FW,ME Fit
I2C2 SCL/SDA netname	SML1_CLK	SML1_DATA	
To where	PMC		
Address	0x23	0x27	Set in PD FW,ME Fit Set in PD FW,ME Fit
I2C3 SCL/SDA netname	I2C3_CLK_PD	I2C3_DATA_PD	
To where	BB		
Address	0x57	0x56	Set in PDFW, BBFW(as default address) Set in PDFW, BBFW(as default address)
PMC to BB's I2C	SML0_CLK	SML0_DATA	
Address	0x55	0x56	Set in PDFW, BBFW(as default address) Set in PDFW, BBFW(as default address)

EC	net name	PD PA_CC1 TBTC	PD PB_CC1 TBTB
GPIO125/I2C07_SDA	I2C3_DATA_PD	0x20	0x24
GPIO124/I2C07_SCL	I2C3_CLK_PD	0x20	0x24





TABLE

LEVEL	MEMORY ID				
	4	3	2	1	0
	R0910	R0911	R0912	R0913	R0914
1	NA	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM	ASM

TABLE:

MEMORYID[4:0]	U2501,U2601,U2701,U2801				Total Memory	LCFC PN
	Supplier	Supplier's P/N	Capacity			
00h (00000b)	SK hynix	H9JCNNNBK3MLYR-N6E	16Gbit	DDP	8GB	SA0000BY300
04h (00100b)		H9JCNNNCP3MLYR-N6E	32Gbit	QDP	16GB	SA0000BL700
08h (01000b)		H9JCNNNFA5MLYR-N6E	64Gbit	ODP	32GB	SA0000BL900
	Samsung		16Gbit	SDP	8GB	
0Ch (01100b)		K3LKBKB0BM-MGCP	32Gbit	DDP	16GB	SA0000BY600
10h (10000b)		K3LKCKC0BM-MGCP	64Gbit	QDP	32GB	SA0000BY700
14h (10100b)	Micron	MT62F512M32D2DR-031	16Gbit	DDP	8GB	SA0000BY500
18h (11000b)		MT62F1G32D4DR-031	32Gbit	QDP	16GB	SA0000BL400
1Ch (11100b)		MT62F2G32D8DR-031	64Gbit	8DP	32GB	SA0000BL600

TABLE

LEVEL	Series ID	
	1	0
	R0927	R0926
1	T	ThinkPAD
0	Ts/X	NEC

TABLE

LEVEL	PLANAR ID			
	3	2	1	0
	R0906	R0907	R0908	R0909
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3:0]
EVT	0000b
FVT	0010b
SIT,SIT2	0100b
SIT-R	0101b
SVT	0111b

← LOGIC

Document Number LCFC

Size Custom | Title 009_CPU(5/16): ESPI/SPI/SMBUS/I3C | Rev 1.0

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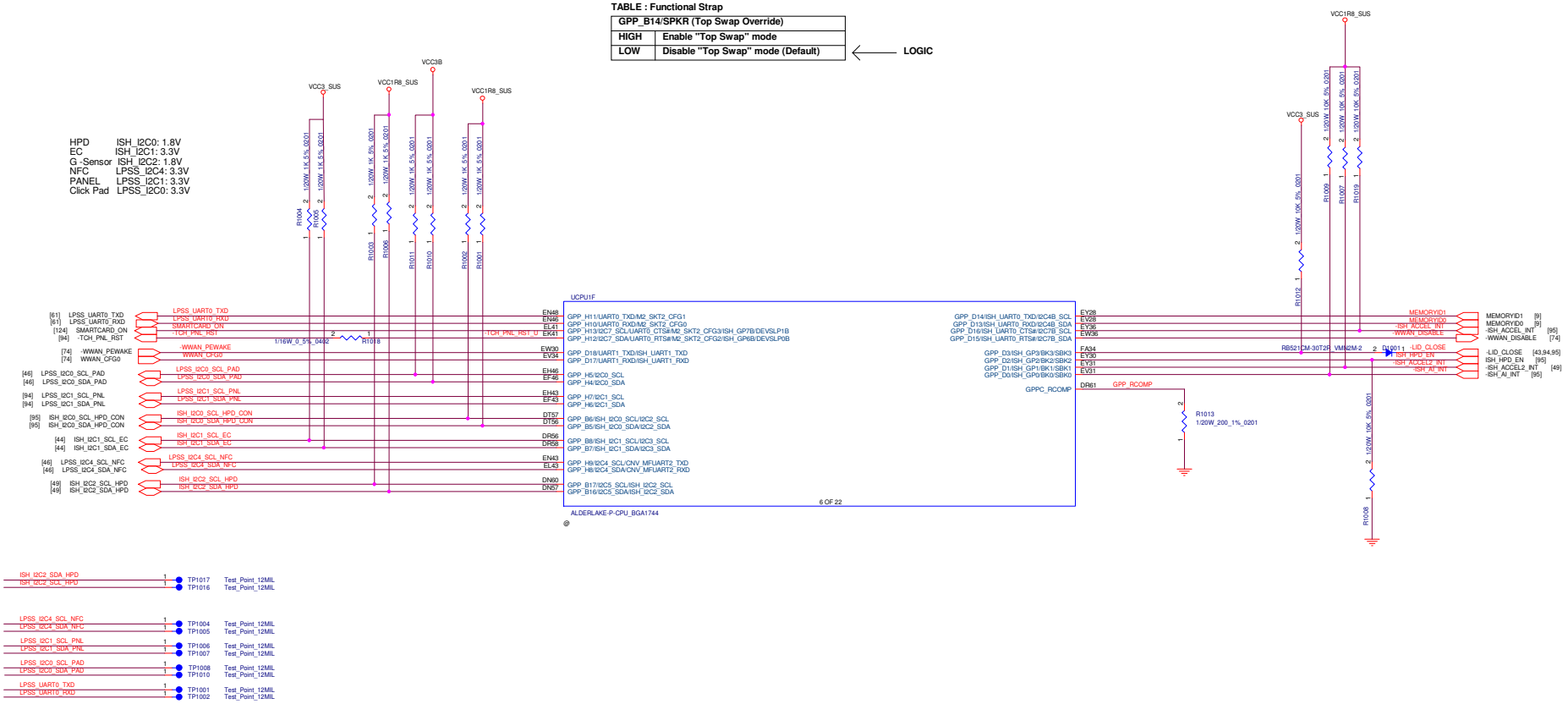
TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default)

← LOGIC

HPD ISH_I2C0: 1.8V
EC ISH_I2C1: 3.3V
G -Sensor ISH_I2C2: 1.8V
NFC LPSS_I2C4: 3.3V
PANEL LPSS_I2C1: 3.3V
Click Pad LPSS_I2C0: 3.3V



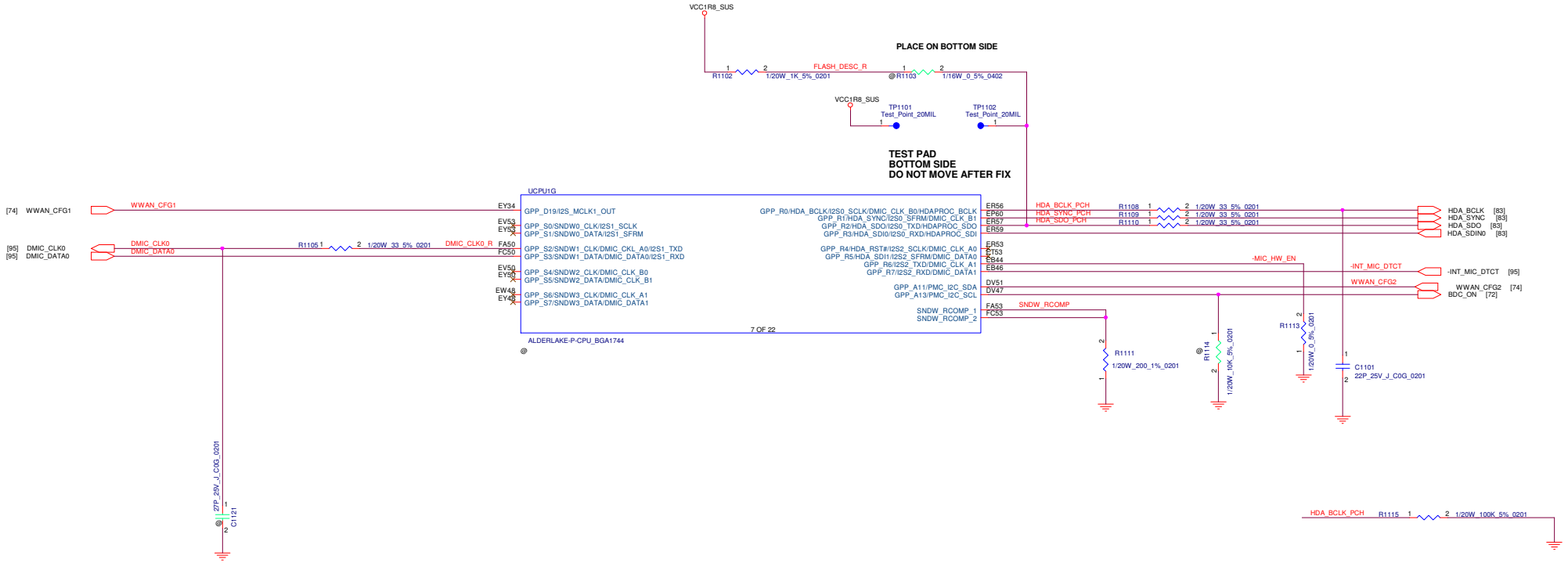
PLACE ON BOTTOM SIDE

LPSS Port Assignment	
LPSS_I2C0	ClickPad
LPSS_I2C1	Touch Panel
ISH_I2C2	G-Sensor
ISH_I2C1	EC
LPSS_I2C4	NFC
ISH_I2C0	HPD
UART0	
UART1	
UART2	
GSPI0	
GSPI1	
GSPI2	

Document Number		LCFC	
Size: Custom	Title: 010_CPU(6/16): LPSS/ISH		Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 10 of 130		

TABLE : Functional Strap

GPP_R2/HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



Document Number			LCFC
Size: Custom	Title: 011_CPU(7/16): AUDIO		Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 11 of 130		

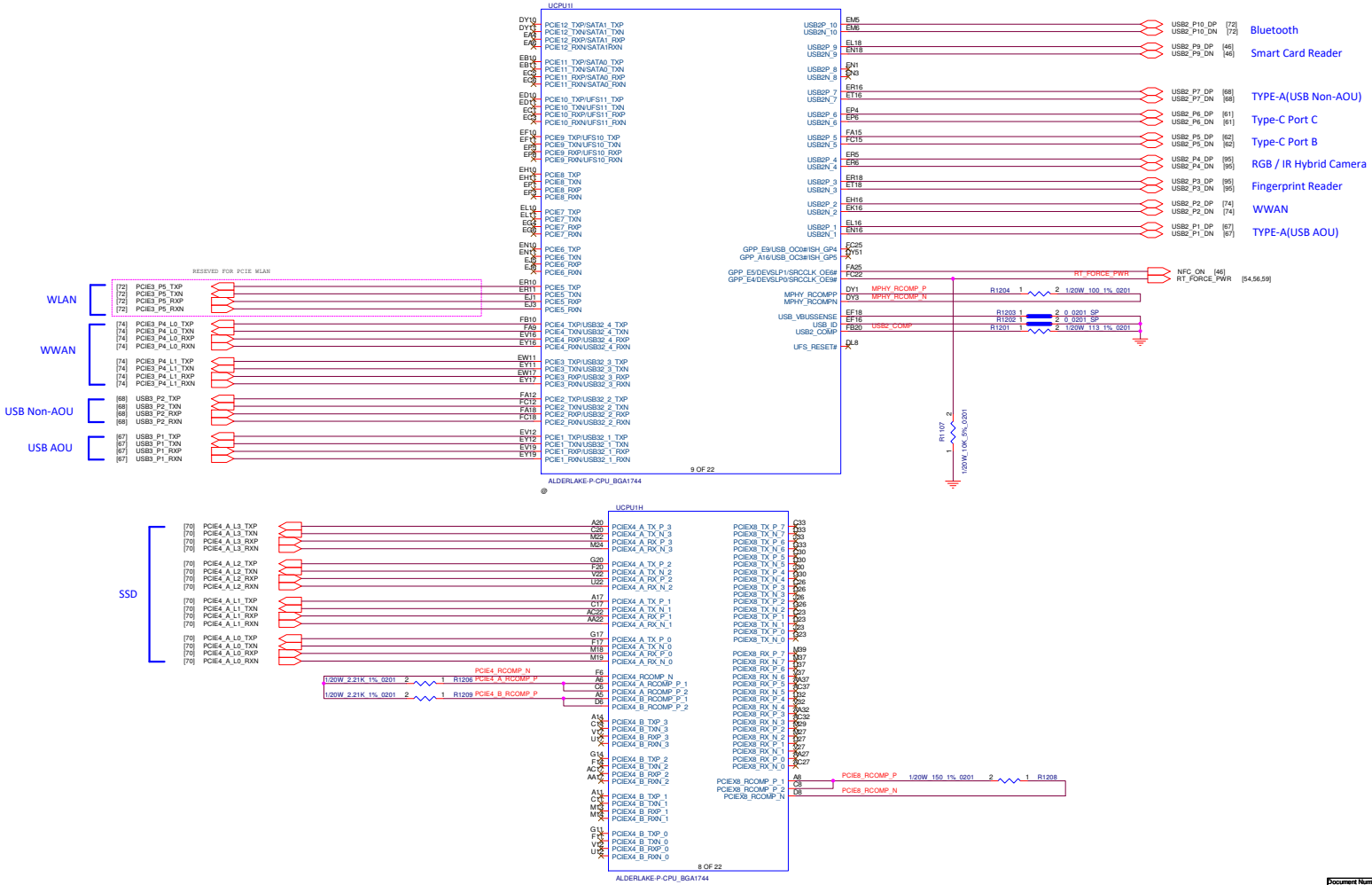
Flexible I/O Configuration							
HSIO Port	High Speed Signals	PCI Device	PCI Function	HSIO Configuration	Descriptor for PCIe	Net Name	PCI Device	PCI Function
PCH L0	USB 3.2 #1 / PCIe Gen3 #1	1Ch	0h	USB 3.2 #1	1x2, 2x1 Lane Reversal Enabled	USB3_P1		
PCH L1	USB 3.2 #2 / PCIe Gen3 #2		1h	USB 3.2 #2		USB3_P2		
PCH L2	USB 3.2 #3 / PCIe Gen3 #3		2h	PCIe Gen3 #3		PCIE3_P4_L1		
PCH L3	USB 3.2 #4 / PCIe Gen3 #4		3h	PCIe Gen3 #4		PCIE3_P4_L0		
PCH L4	PCIe Gen3 #5	1Ch	4h	PCIe Gen3 #5	4x1 Lane Reversal Disabled	PCIE3_P5		
PCH L5	PCIe Gen3 #6		5h	PCIe Gen3 #6		N/A		
PCH L6	PCIe Gen3 #7 (GbE)		6h	PCIe Gen3 #7 (GbE)		N/A		
PCH L7	PCIe Gen3 #8 (GbE)		7h	PCIe Gen3 #8		N/A		
PCH L8	PCIe Gen3 #9 (GbE)	1Dh	0h	PCIe Gen3 #9 (x4)	1x4 Lane Reversal Disabled	N/A		
PCH L9	PCIe Gen3 #10		1h	PCIe Gen3 #10 (x4)		N/A		
PCH L10	PCIe Gen3 #11 / SATA #0		2h	PCIe Gen3 #11 (x4)		N/A		
PCH L11	PCIe Gen3 #12 / SATA #1		3h	PCIe Gen3 #12 (x4)		N/A		
CPU L0	PCIe Gen4 x4Lane 0	06h	0h	PCIe Gen4 (x4) L0	1x4 Lane Reversal Disabled	PCIE4_L0		
CPU L1	PCIe Gen4 x4Lane 1			PCIe Gen4 (x4) L1		PCIE4_L1		
CPU L2	PCIe Gen4 x4Lane 2			PCIe Gen4 (x4) L2		PCIE4_L2		
CPU L3	PCIe Gen4 x4Lane 3			PCIe Gen4 (x4) L3		PCIE4_L3		

PCIe Port Assignment	
PCIE3_P1	(USB3_P1)
PCIE3_P2	(USB3_P2)
PCIE3_P3	WWAN Lane 1
PCIE3_P4	WWAN Lane 0
PCIE3_P5	(WLAN)
PCIE3_P6	(Reserved)
PCIE3_P7	(Reserved)
PCIE3_P8	(Reserved)
PCIE3_P9 (x4)	(Reserved)
PCIE4 (x4)	NVMe SSD

SATA Port Assignment	
SATA_P0	(PCIE3_P11)
SATA_P1	(PCIE3_P12)

USB 3.2 Port Assignment	
USB3_P1	Type-A Port(AOU)
USB3_P2	Type-A Port (non-AOU sub/B)
USB3_P3	(PCIE3_P3)
USB3_P4	(PCIE3_P4)

USB 2.0 Port Assignment	
USB2_P1	Type-A Port(AOU)
USB2_P2	WWAN
USB2_P3	Fingerprint Reader
USB2_P4	RGB / IR Hybrid Camera
USB2_P5	Type-C Port A
USB2_P6	Type-C Port C
USB2_P7	Type-A Port (non-AOU Sub/B)
USB2_P8	(Reserve)
USB2_P9	(Smart Card Reader)
USB2_P10	(Bluetooth)



Document Number			LCFC	
Size: Custom	Title: 012_CPU(8/16): PCIE/USB/SATA			Rev: A01
Date: Tuesday, January 04, 2022	Sheet 12 of 130			

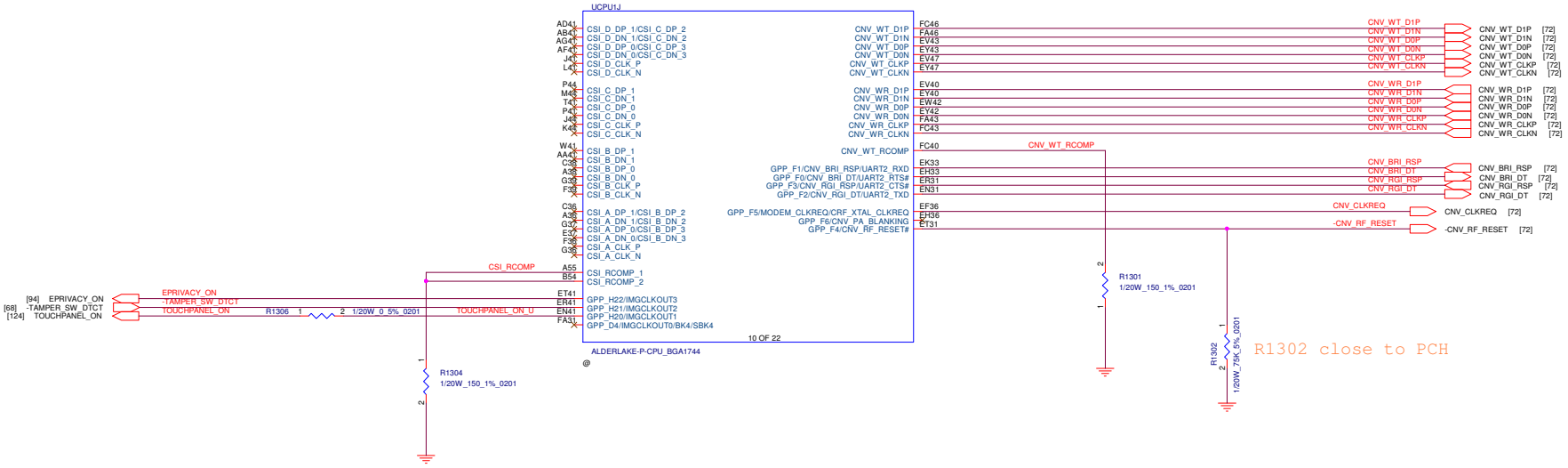


TABLE : Functional Strap

GPP_F2/CNV_RGI_DT(M.2 CNVi Mode Select)	
HIGH	Integrated CNVi Disabled
LOW	Integrated CNVi Enabled

← LOGIC

TABLE : Functional Strap

GPP_F0/CNV_BRI_DT (XTAL Frequency Selection)	
HIGH	24MHz XTAL selected
LOW	38.4MHz XTAL frequency selected (Default)

← LOGIC

[Issue Symptom]
All PCIe device can't recognize

[Root cause]
GPP_F0 strap not correct setting.

[Solution]
GPIO need to set up "native" and can't have PU resistance.

Interface	Ball Number	Pin Name	Board Rterm (Ohm)	Board DC resistance (ohms)	Board parasitic capacitance (pF)	Notes
PCH interface	FC40	CNV_WT_RCOMP	150 ohm +/-1 % pull-down to GND	<0.5	-	Pkg trace + Board trace <1pF should be sufficient

Document Number		LCFC	
Size: Custom	Title: 013_CPU(9/16): CSI-2/CNVI		Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 13 of 130		

PCIECLK and CLKREQ# Port Assignment		
Port 0	PCIe Gen4 A(x4)	NVMe SSD
Port 1	PCIe Gen3 P5	(M.2 WLAN)
Port 2	PCIe Gen3 P1	M.2 WWAN
Port 3	PCIe Gen4 B (x4)	(Reserved)
Port 4	PCIe Gen3 P7	(Reserved)
Port 5	PCIe Gen3 P8	(Reserved)
Port 6	PCIe Gen3 P6	(Reserved)

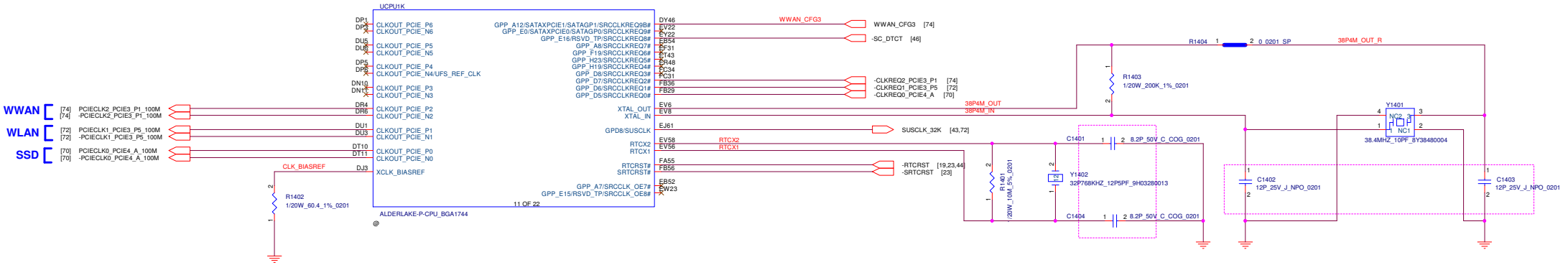


TABLE of Y1402		
Vendor	P/N	LCFC P/N
EPSON	X1A000141000200	SJ10000IX00
TXC	9H03280012	SJ10000J900
TKD	SF32K32768D91T-V	SJ10000WR00

TABLE of Y1401		
Vendor	P/N	LCFC P/N
TXC	8Y38480004	SJ10000SN00
TXC	7R38400001	SJ10000RU00
KDS	7AF03840A04	SJ10000XG00

Document Number			LCFC
Size: Custom	Title: 014_CPU(10/16): CLOCK SIGNALS		Rev: V05
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TABLE : U1501

TI	SN74LVC1G17DRLR	SA00005MG00
TOSHIBA	TC7SZ17FE	SA00008EZ00
ONSemi	NL17SZ17XV5T2G	SA00005OU00

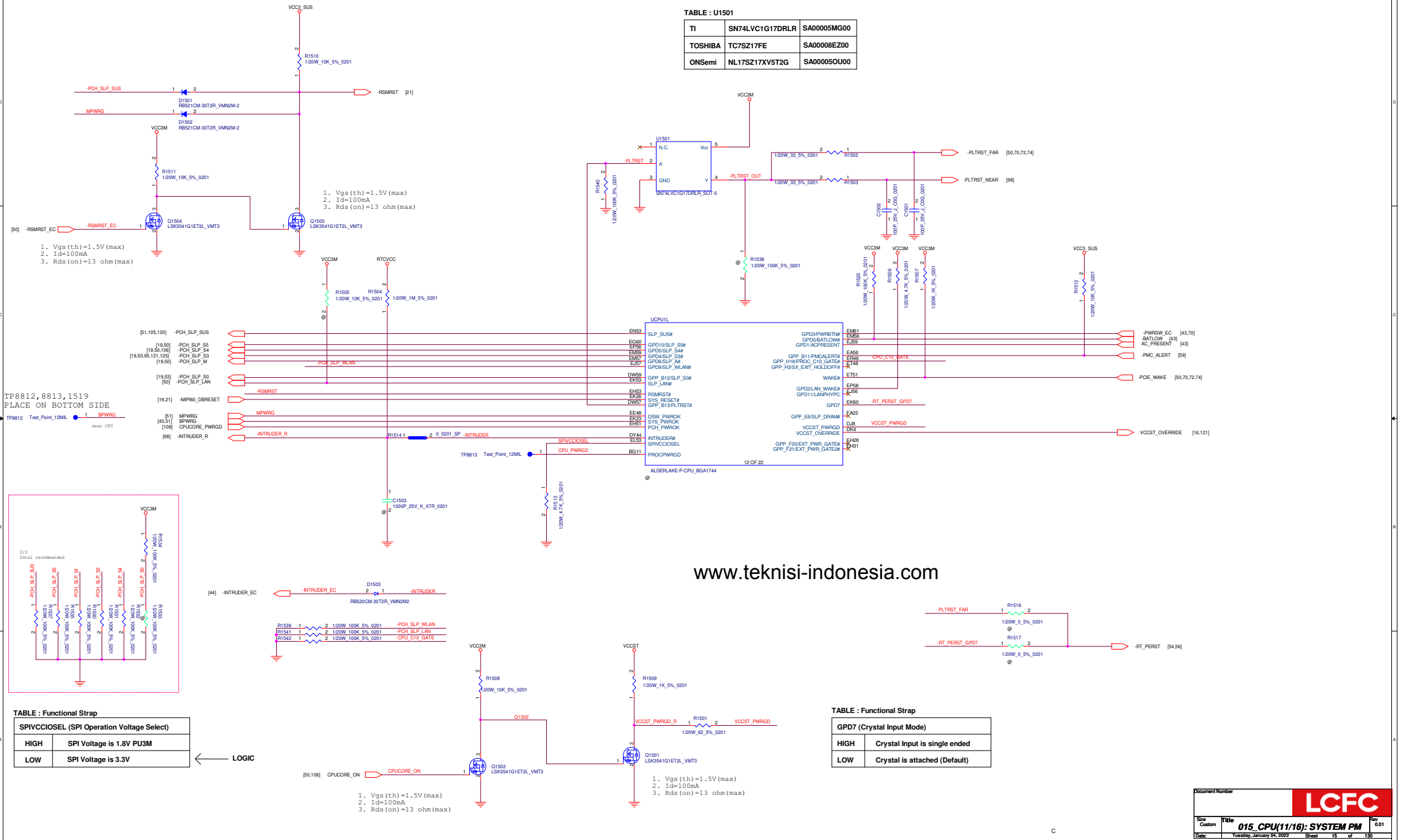

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TABLE : Functional Strap

SPIVCCIOSEL (SPI Operation Voltage Select)	
HIGH	SPI Voltage is 1.8V PU3M
LOW	SPI Voltage is 3.3V

LOGIC

TABLE : Functional Strap

GPD7 (Crystal Input Mode)	
HIGH	Crystal Input is single ended
LOW	Crystal is attached (Default)

Document Number		LCFC	
Size: Custom	Title: 015_CPU(11/16): SYSTEM PM		Rev: 0.01
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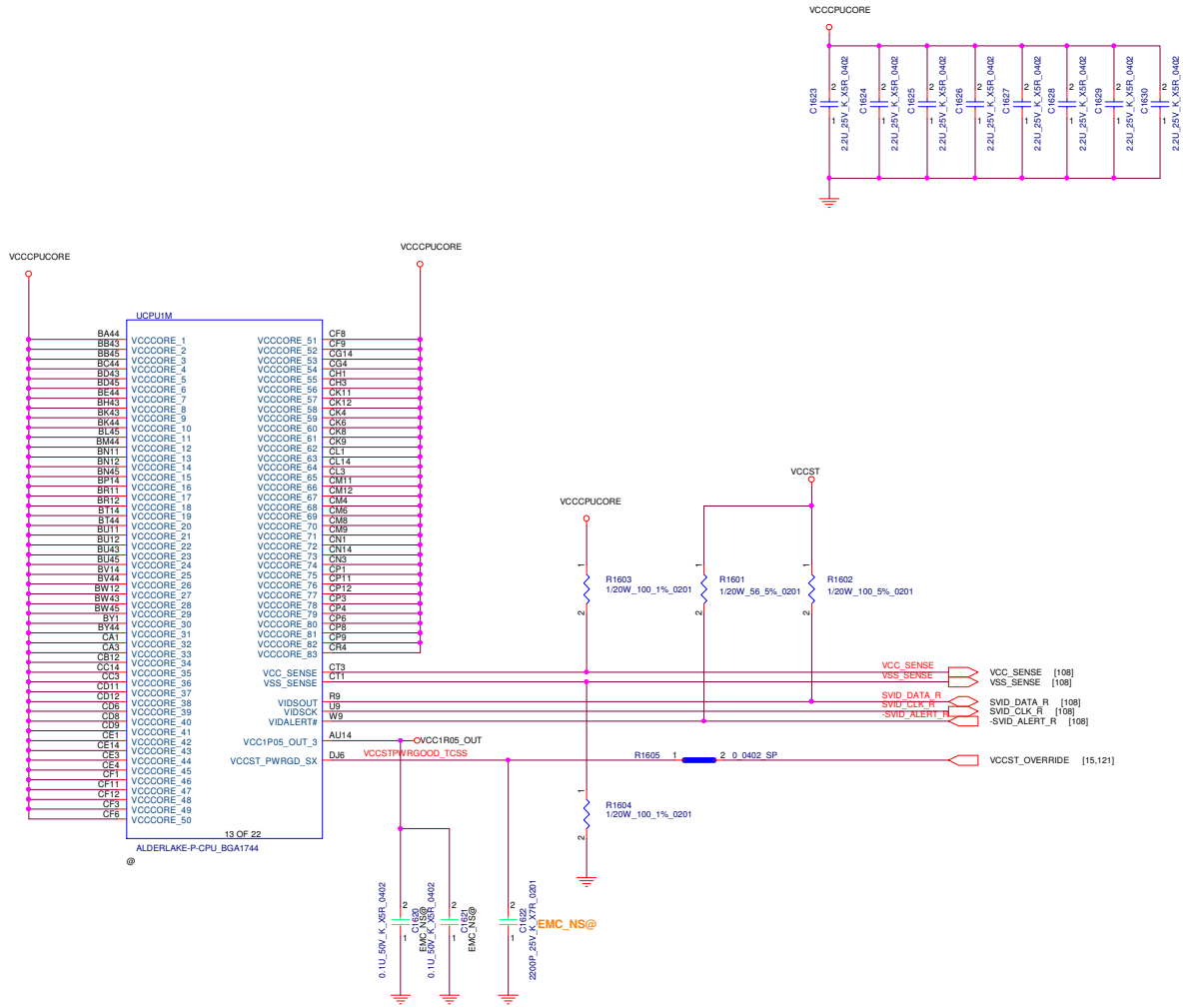

Document Number		LCFC
Size: Custom	Title: 016_CPU(12/16): CPU POWER (1/2)	Rev
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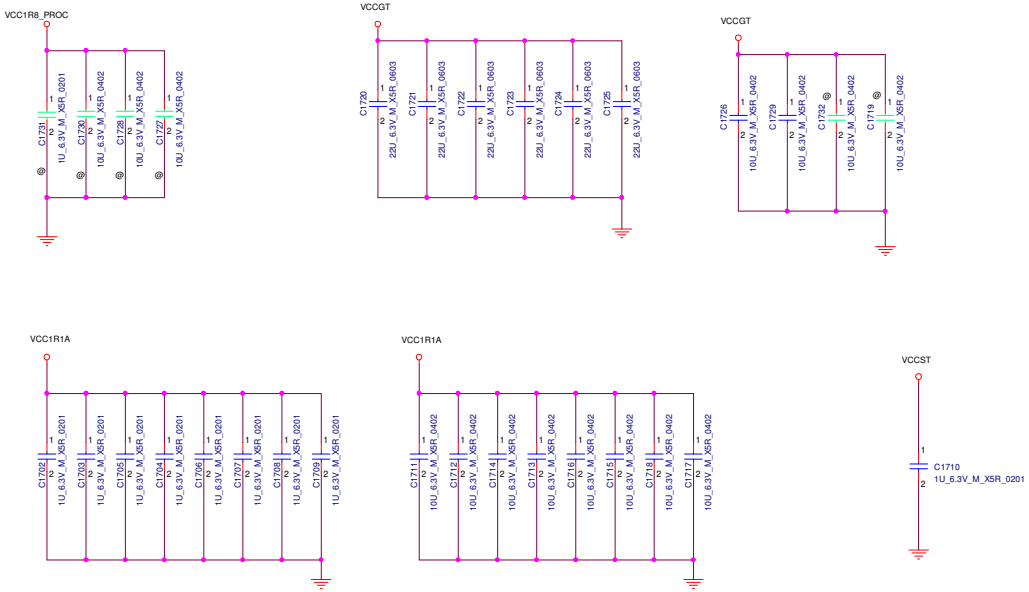
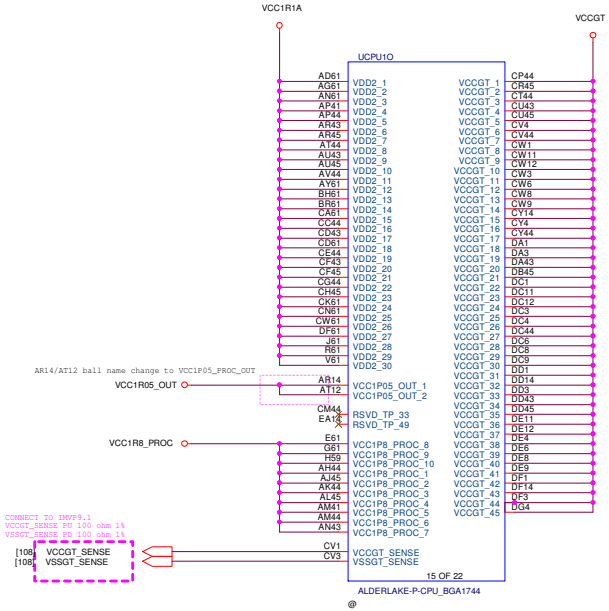
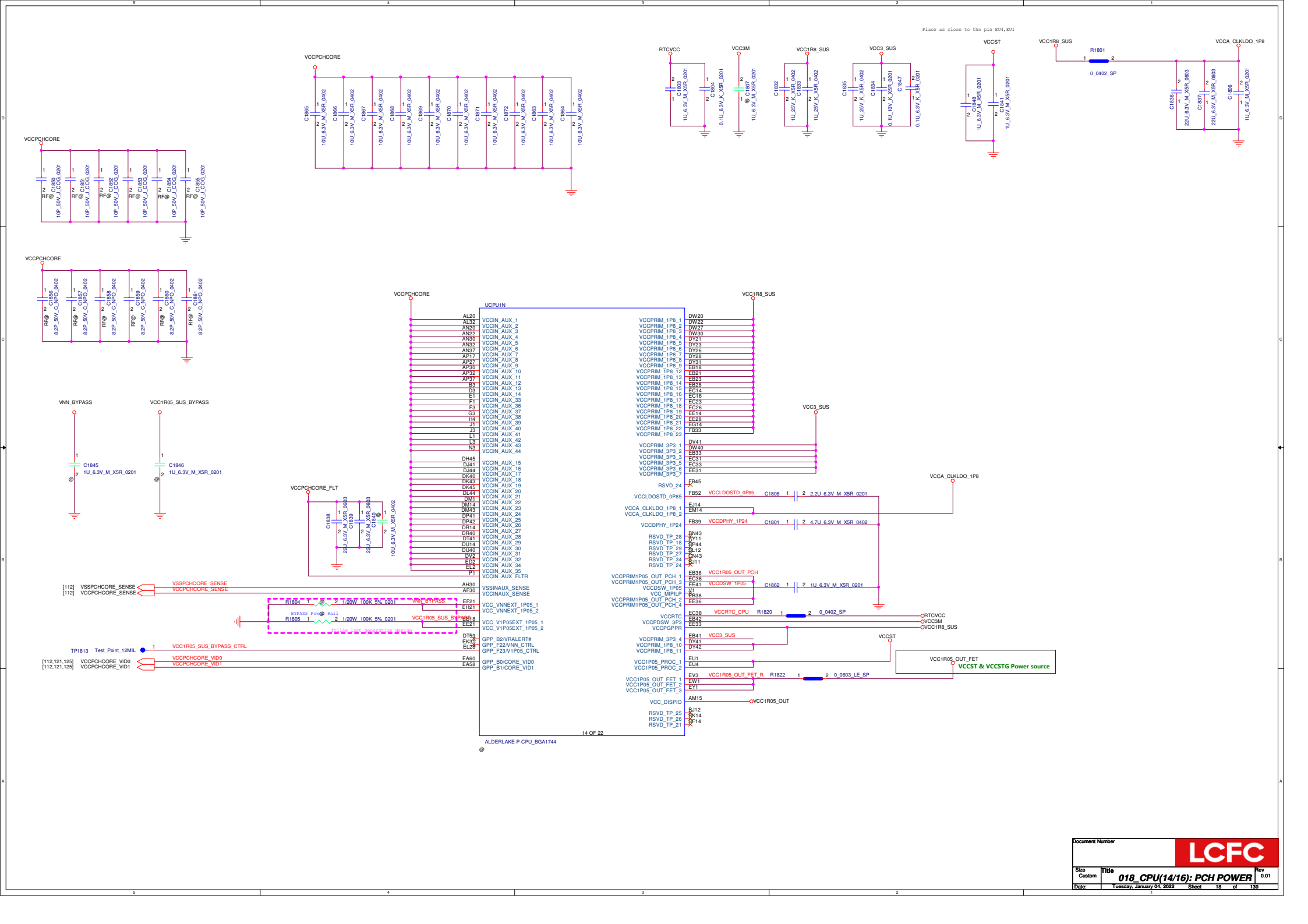




Document Number	LCFC
Size: Custom	Title: 017_CPU(13/16): CPU POWER(2/2)
Rev	
Date: Tuesday, January 04, 2022	Sheet 17 of 130



Document Number			LCFC
Size: Custom	Title: 018_CPU(14/16): PCH POWER		Rev: 0.01
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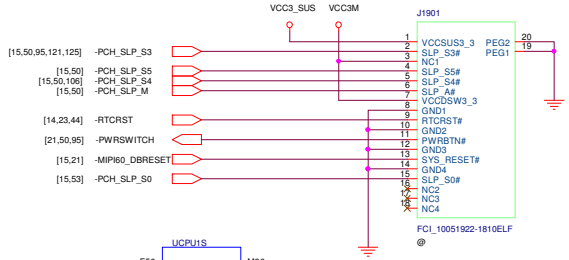
APS/PETS Interface



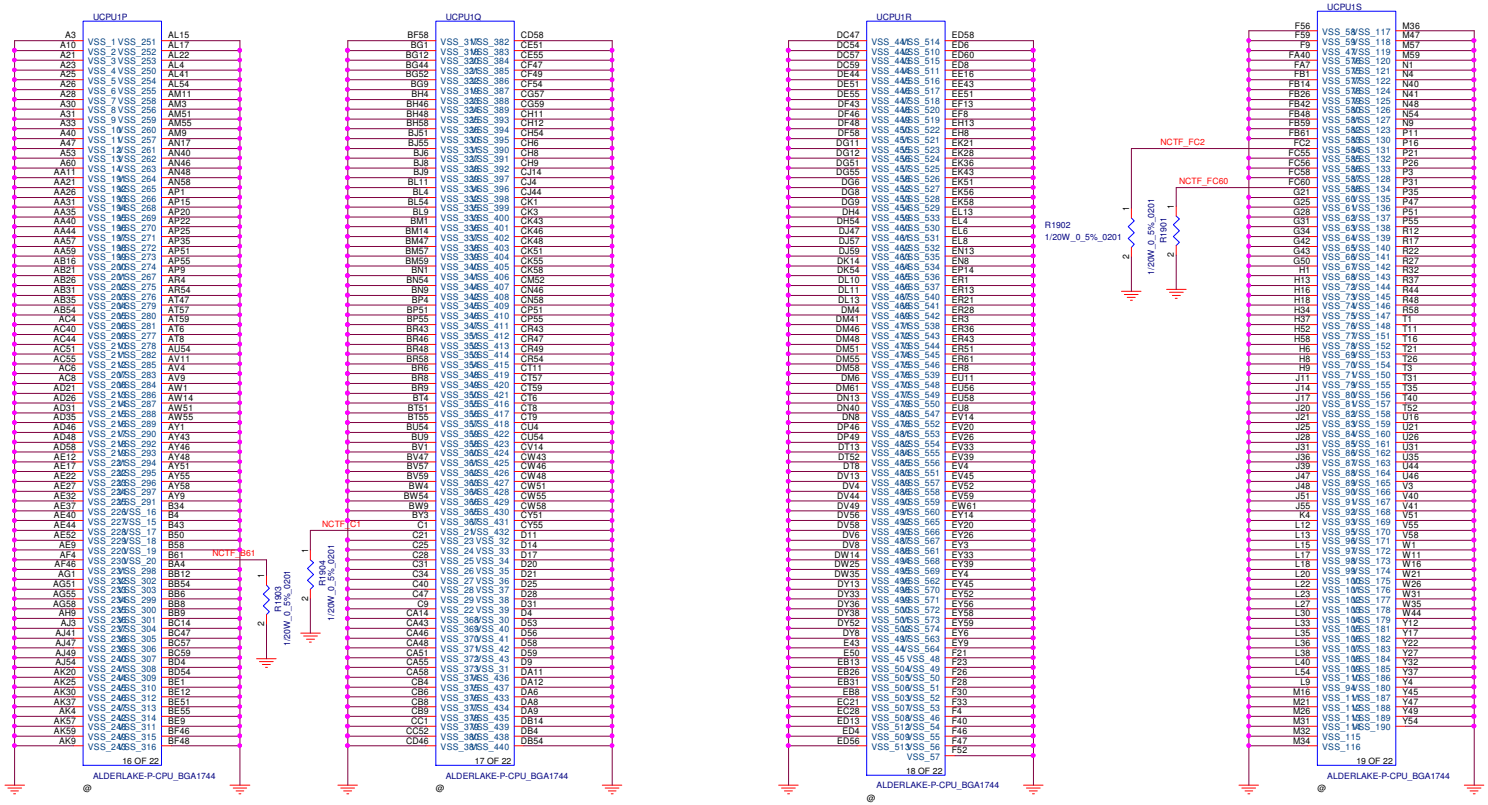


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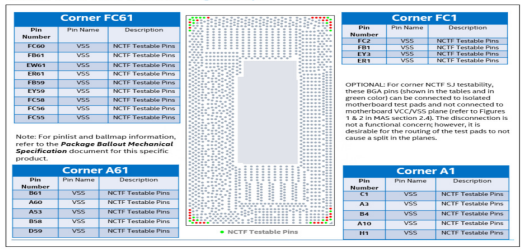
Figure 13. Corner NCTF Test- PCB Routing Example



Refer Alder Lake P Processor Line BGA Package Ball out Mechanical Specification document # 627000 for Pin details

Document Number			
Size: Custom	Title: 019_CPU(15/16): GND		Rev: 0.01
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5.7 CFG Signals Functionality and Termination

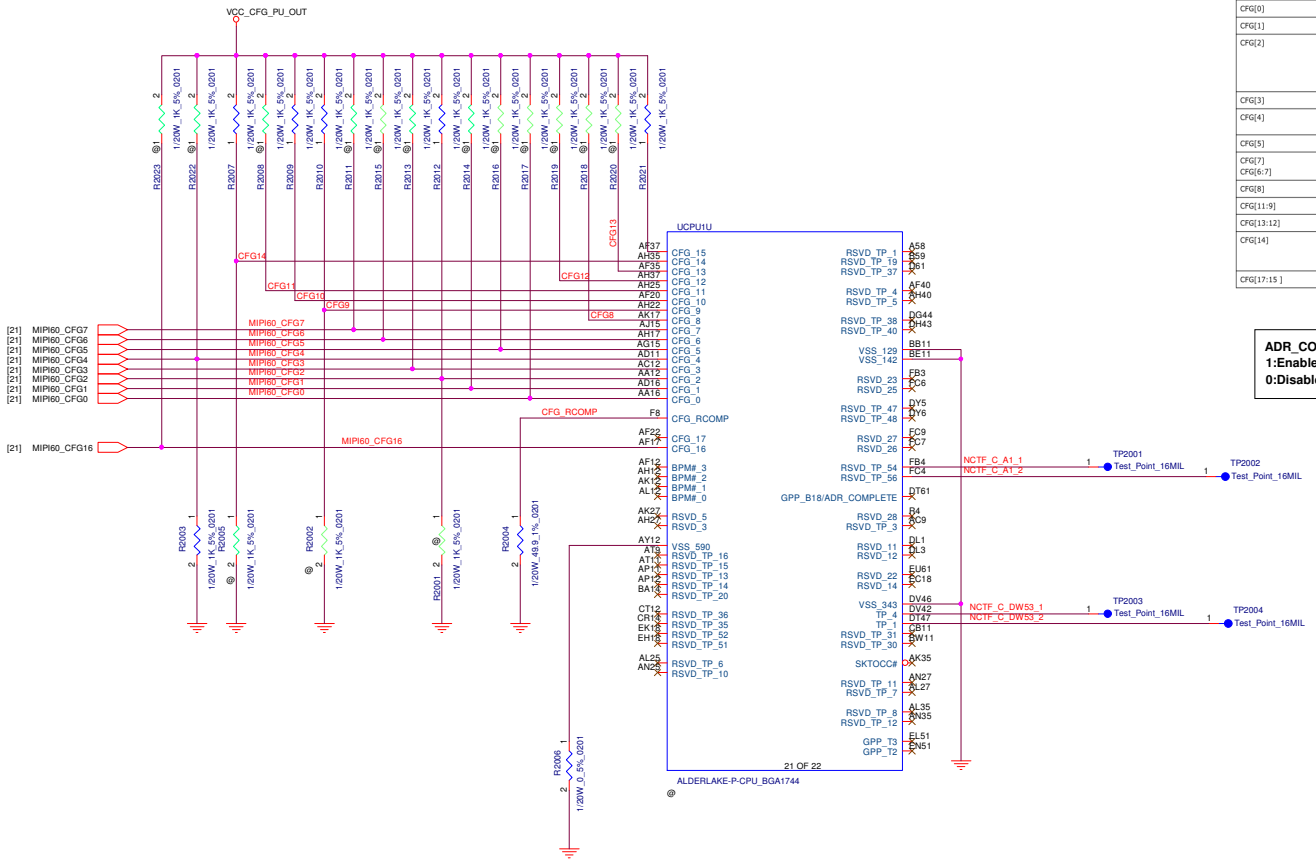
Table 343. CFG Signals Functionality and Termination

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull -Up to VCC_CFG_PU_OUT	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	none	
CFG[2]	PCI Express* Static X8 Lane Numbering Reversal • 1:Normal Operation • 0: Lane Numbers reversed	Pull -Up to VCC_CFG_PU_OUT	1K ohm
CFG[3]	RSVD	None	
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull -Up to VCC_CFG_PU_OUT	1K ohm
CFG[5]	RSVD	None	
CFG[7] CFG[6:7]	RSVD	None	
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	None	
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull-up to VCC_CFG_PU_OUT	1K ohm
CFG[17:15]	RSVD	None	

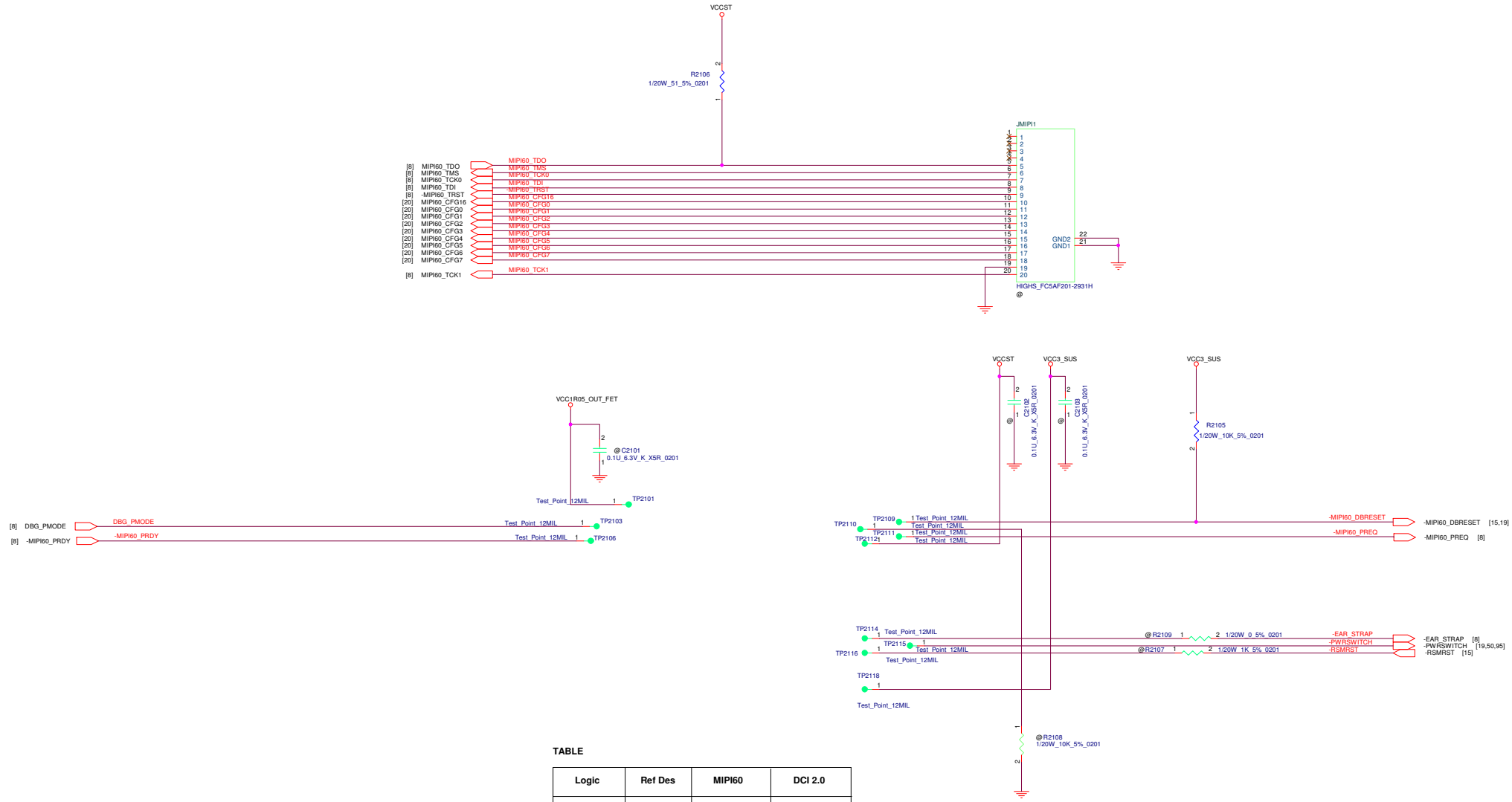
TABLE

CFG3: MSR Privacy Bit Feature **1: MSR (C80h) bit[0] setting** **0: MSR (C80h) bit[0] overridden**
CFG4: eDP Enable **1:Disabled** **0:Enabled**
CFG9: SVID Bus Communication **1:Enabled** **0:Disabled**
CFG14: PEG60 Lane Reversal **1:Normal** **0:Reversed**

ADR_COMPLETE
1:Enabled NO REBOOT
0:Disabled REBOOT ENABLED



Document Number			LCFC
Size: Custom	Title: 020_CPU(16/16): CFG/RESERVED		Rev: 1.01
Date: Tuesday, January 04, 2022	Sheet 20 of 130		



TABLE

Logic	Ref Des	MIPI60	DCI 2.0
Page8	R0808	ASM	NO_ASM
	R0809	ASM	NO_ASM
Page 20	R2001	ASM	NO_ASM
Page 22	J8	ASM	NO_ASM
	C2101	ASM	NO_ASM
	C2102	ASM	NO_ASM
	C2103	ASM	NO_ASM
	R2108	ASM	NO_ASM
	R2106	ASM	ASM
	R2105	ASM	ASM
	R2104	ASM	NO_ASM
	R2107	ASM	NO_ASM
	R2109	ASM	NO_ASM

LOGIC

Lenovo

Project Name : T14s Gen2	Title : MIPI60 DEBUG PORT
Size : C	Document Number :
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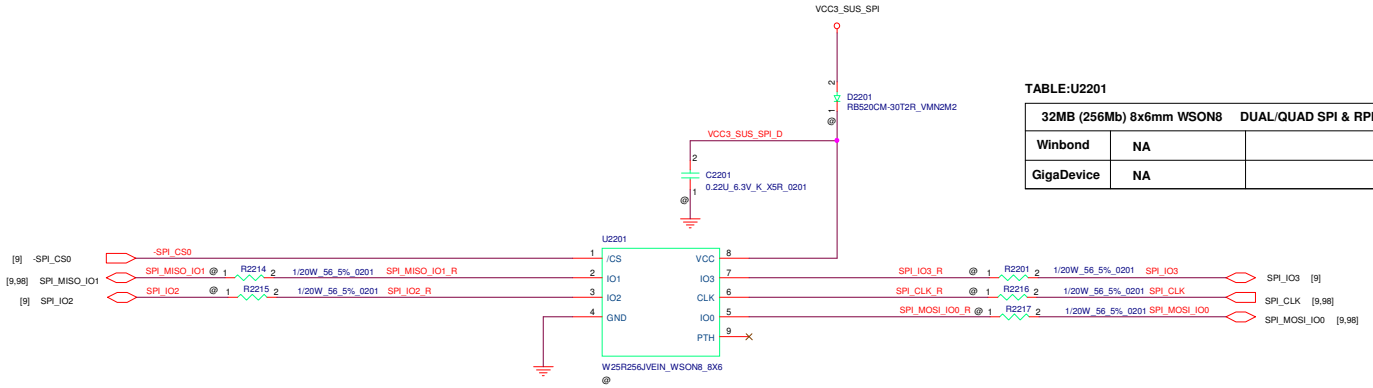
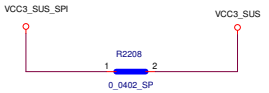


TABLE:U2201

32MB (256Mb) 8x6mm WSON8	DUAL/QUAD SPI & RPMC	
Winbond	NA	
GigaDevice	NA	



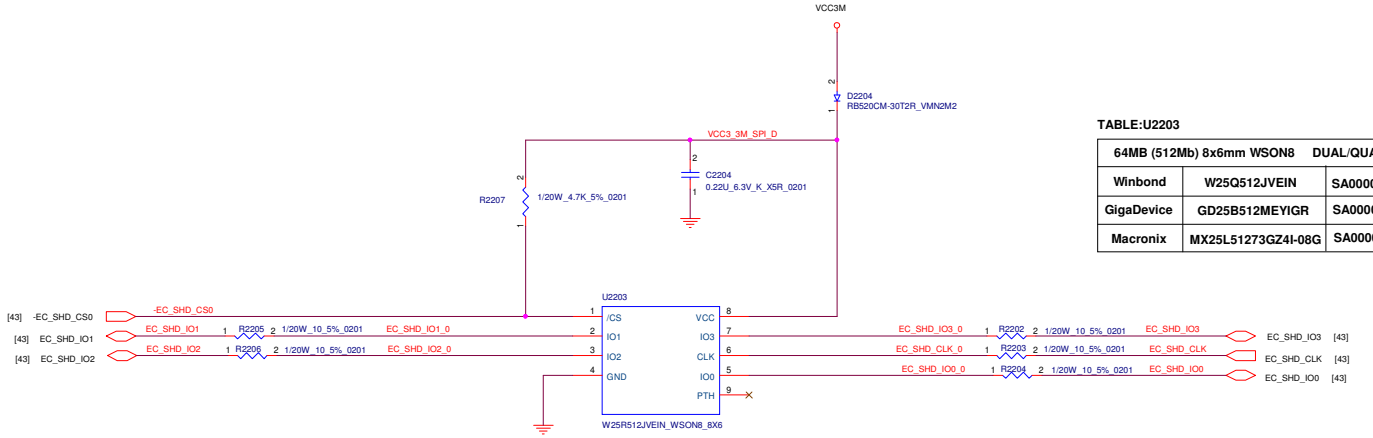
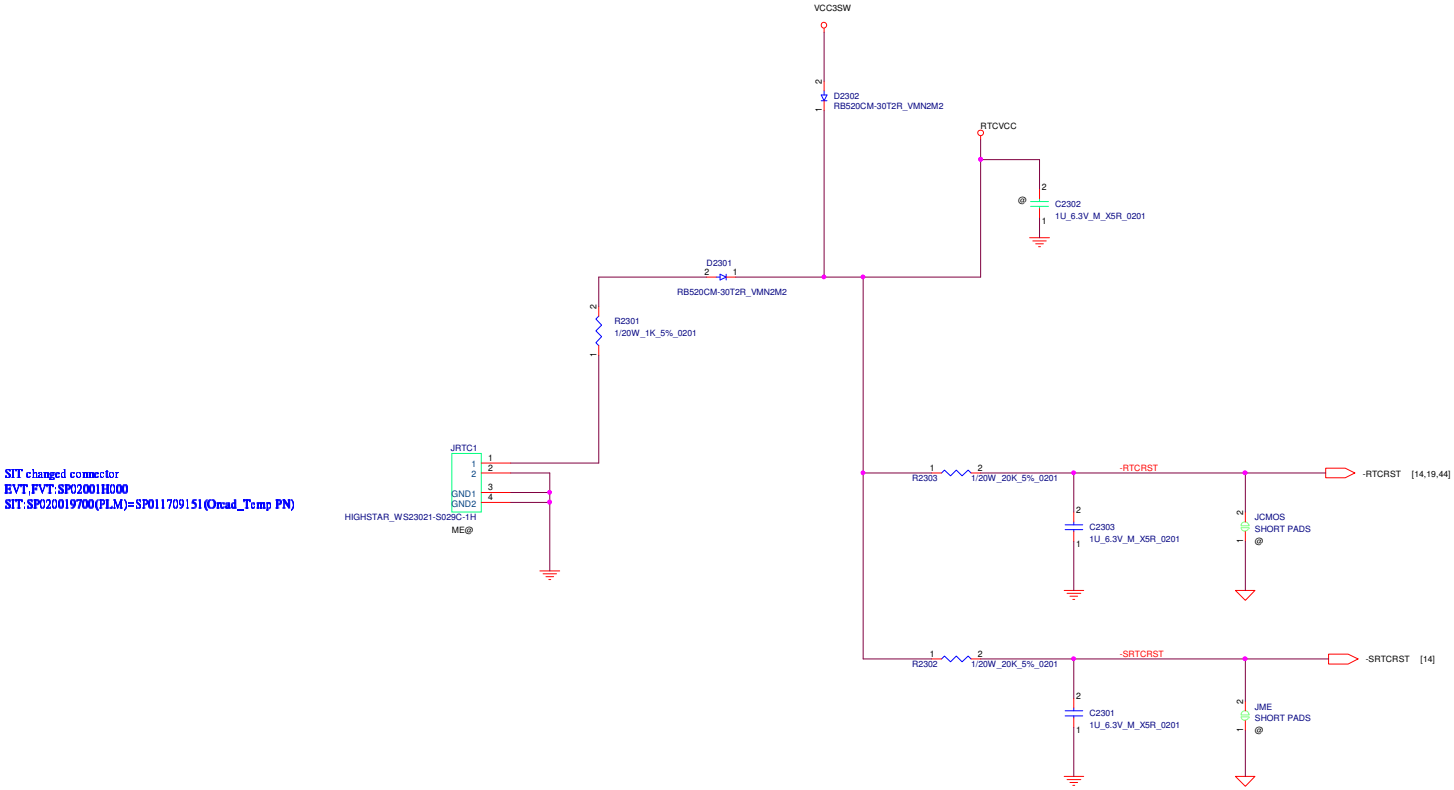


TABLE:U2203

64MB (512Mb) 8x6mm WSON8		DUAL/QUAD SPI & RPMC
Winbond	W25Q512JVEIN	SA0000BUN00
GigaDevice	GD25B512MEYIGR	SA0000BV300
Macronix	MX25L51273GZ4I-08G	SA0000CDT00

Document Number		LCFC
Size: Custom	Title: 022_SPI FLASH	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 22 of 130	



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Project Name : T14s Gen2	Title : RTC BATTERY	
Size : C	Document Number :	Rev : 0.1
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Title	<Title>		
Size	Document Number		Rev
Custom	T14s Gen2		0.1
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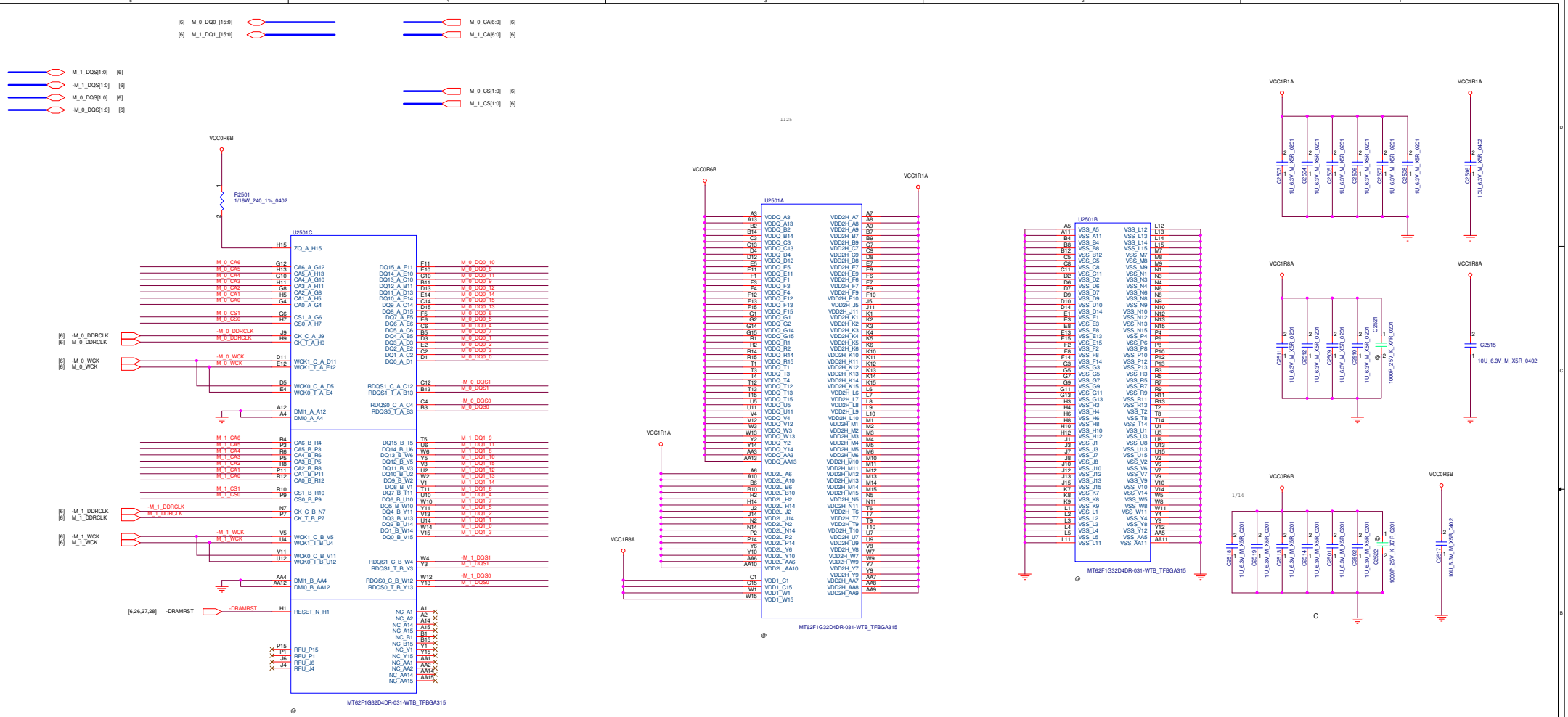

TABLE : LPDDR5 Source

Supplier	Capacity	Supplier's P/N	Package Size		Die	Device Configuration?	Memory
SK Hynix	16Gbit	H9JCNNNBK3MLYR-N6E	12.4 x 15 mm	DDP	8Gb	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	H9JCNNNCP3MLYR-N6E	12.4 x 15 mm	QDP	8Gb	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	H9JCNNNFA5MLYR-N6E	12.4 x 15 mm	ODP	8Gb	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gbit						8GB
	32Gbit	K3LKBKB0BM-MGCP	12.4 x 15 mm	DDP	16Gb	1 Rank x (1Gx16) x 2 Ch	16GB
	64Gbit	K3LKCKC0BM-MGCP	12.4 x 15 mm	QDP	16Gb	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gbit	MT62F512M32D2DR-031	12.4 x 15 mm	DDP	8Gb	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	MT62F1G32D4DR-031	12.4 x 15 mm	QDP	8Gb	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	MT62F2G32D8DR-031	12.4 x 15 mm	ODP	8Gb	2 Rank x (1Gx16) x 2 Ch	32GB

Document Number

LCFC

Size: Custom | Title: 025_LPDDR5 CHANNEL 0&1 | Rev: 0.01

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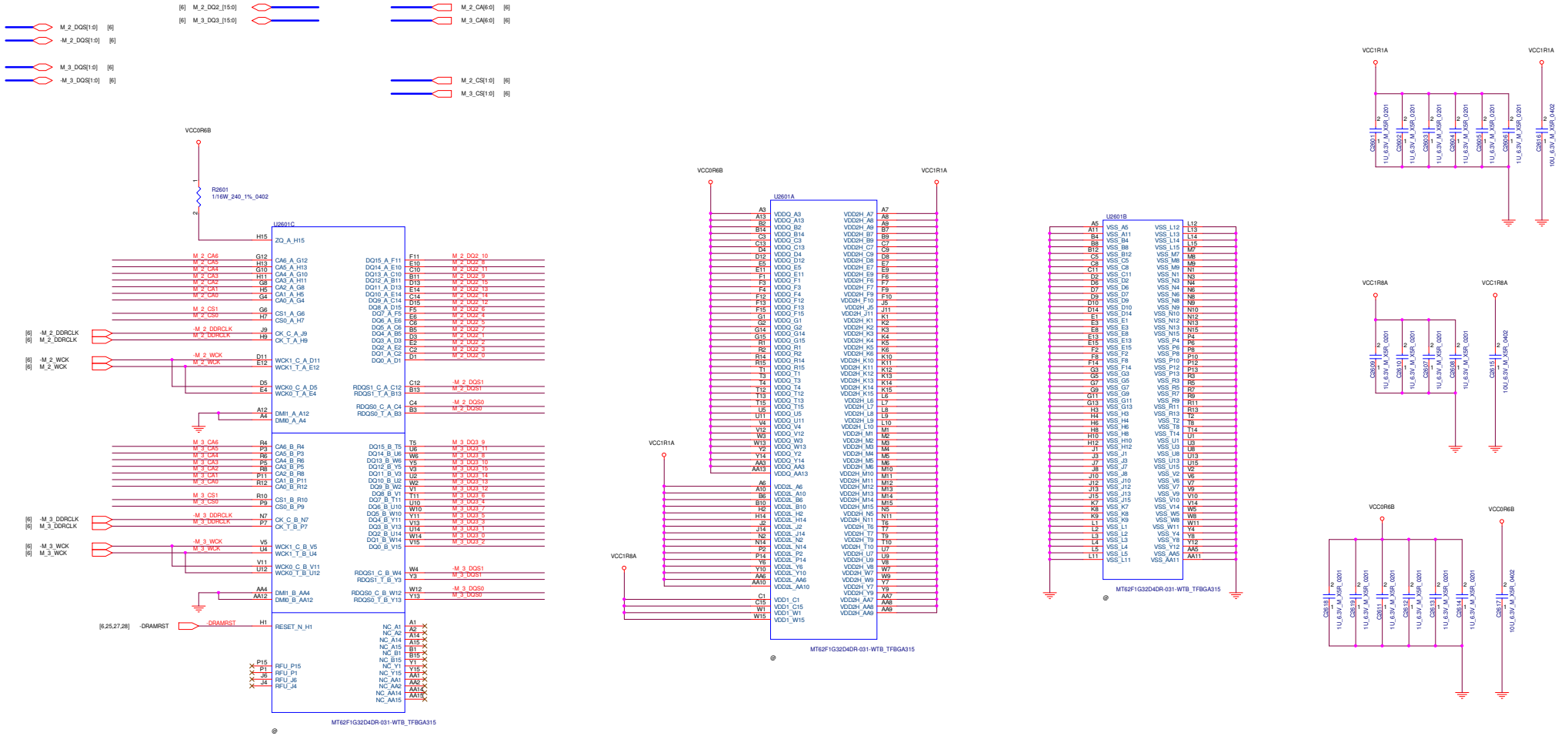

TABLE : LPDDR5 Source

Supplier	Capacity	Supplier's P/N	Package Size		Die	Device Configuration?	Memory
SK Hynix	16Gbit	H9JCNNNBK3MLYR-N6E	12.4 x 15 mm	DDP	8Gb	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	H9JCNNNCP3MLYR-N6E	12.4 x 15 mm	QDP	8Gb	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	H9JCNNNFA5MLYR-N6E	12.4 x 15 mm	ODP	8Gb	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gbit						8GB
	32Gbit	K3LKBKB0BM-MGCP	12.4 x 15 mm	DDP	16Gb	1 Rank x (1Gx16) x 2 Ch	16GB
	64Gbit	K3LKCKC0BM-MGCP	12.4 x 15 mm	QDP	16Gb	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gbit	MT62F512M32D2DR-031	12.4 x 15 mm	DDP	8Gb	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	MT62F1G32D4DR-031	12.4 x 15 mm	QDP	8Gb	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	MT62F2G32D8DR-031	12.4 x 15 mm	ODP	8Gb	2 Rank x (1Gx16) x 2 Ch	32GB

Document Number

LCFC

Size: Custom | Title: 026_LPDDR5 CHANNEL 2&3 | Rev: 0.01

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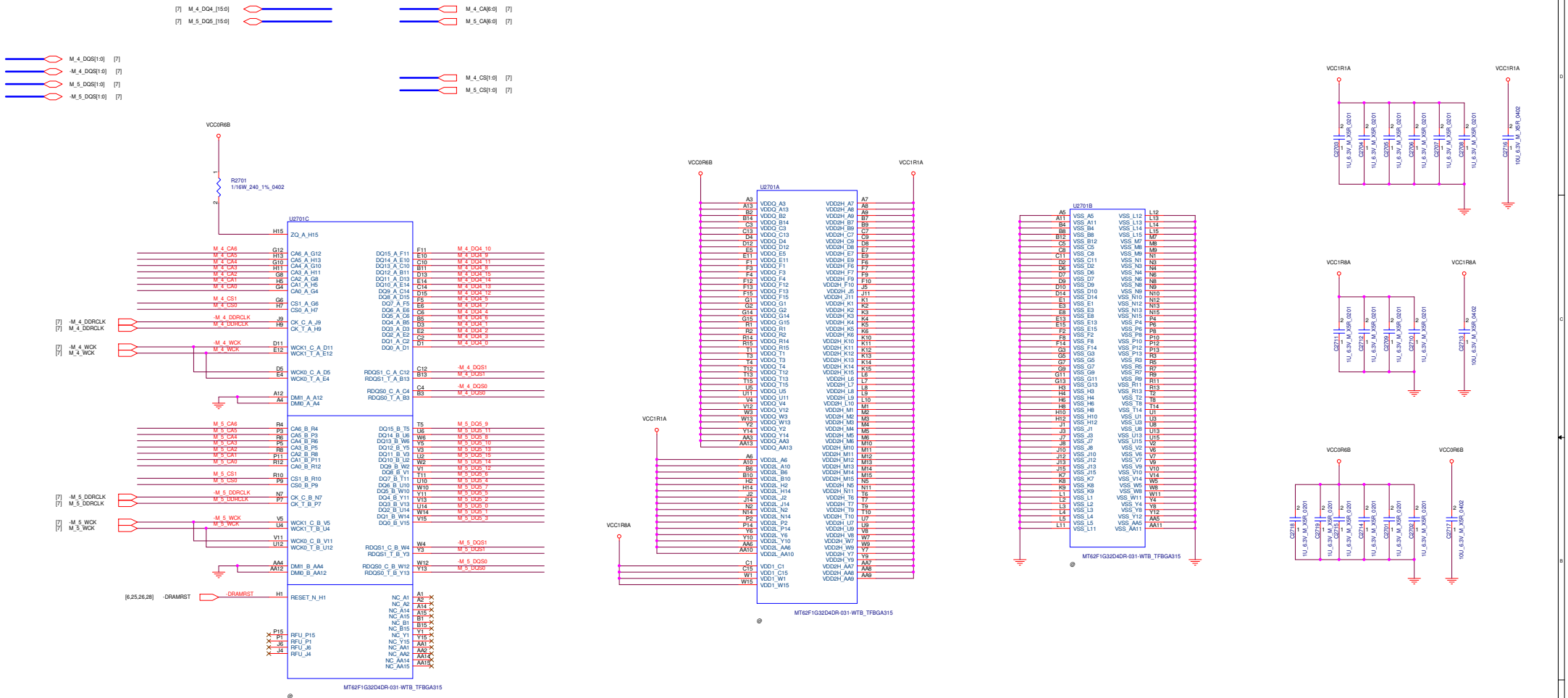

TABLE : LPDDR5 Source

Supplier	Capacity	Supplier's P/N	Package Size		Die	Device Configuration?	Memory
SK Hynix	16Gbit	H9JCNNNBK3MLYR-N6E	12.4 x 15 mm	DDP	8Gb	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	H9JCNNNCP3MLYR-N6E	12.4 x 15 mm	QDP	8Gb	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	H9JCNNNFA5MLYR-N6E	12.4 x 15 mm	ODP	8Gb	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gbit						8GB
	32Gbit	K3LKBKB0BM-MGCP	12.4 x 15 mm	DDP	16Gb	1 Rank x (1Gx16) x 2 Ch	16GB
	64Gbit	K3LKCKC0BM-MGCP	12.4 x 15 mm	QDP	16Gb	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gbit	MT62F512M32D2DR-031	12.4 x 15 mm	DDP	8Gb	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	MT62F1G32D4DR-031	12.4 x 15 mm	QDP	8Gb	2 Rank x (1Gx16) x 2 Ch	16GB
	64Gbit	MT62F2G32D8DR-031	12.4 x 15 mm	ODP	8Gb	2 Rank x (1Gx16) x 2 Ch	32GB

Document Number		LCFC	
Size: Custom	Title: 027_LPDDR5 CHANNEL 4&5		Rev: 0.01
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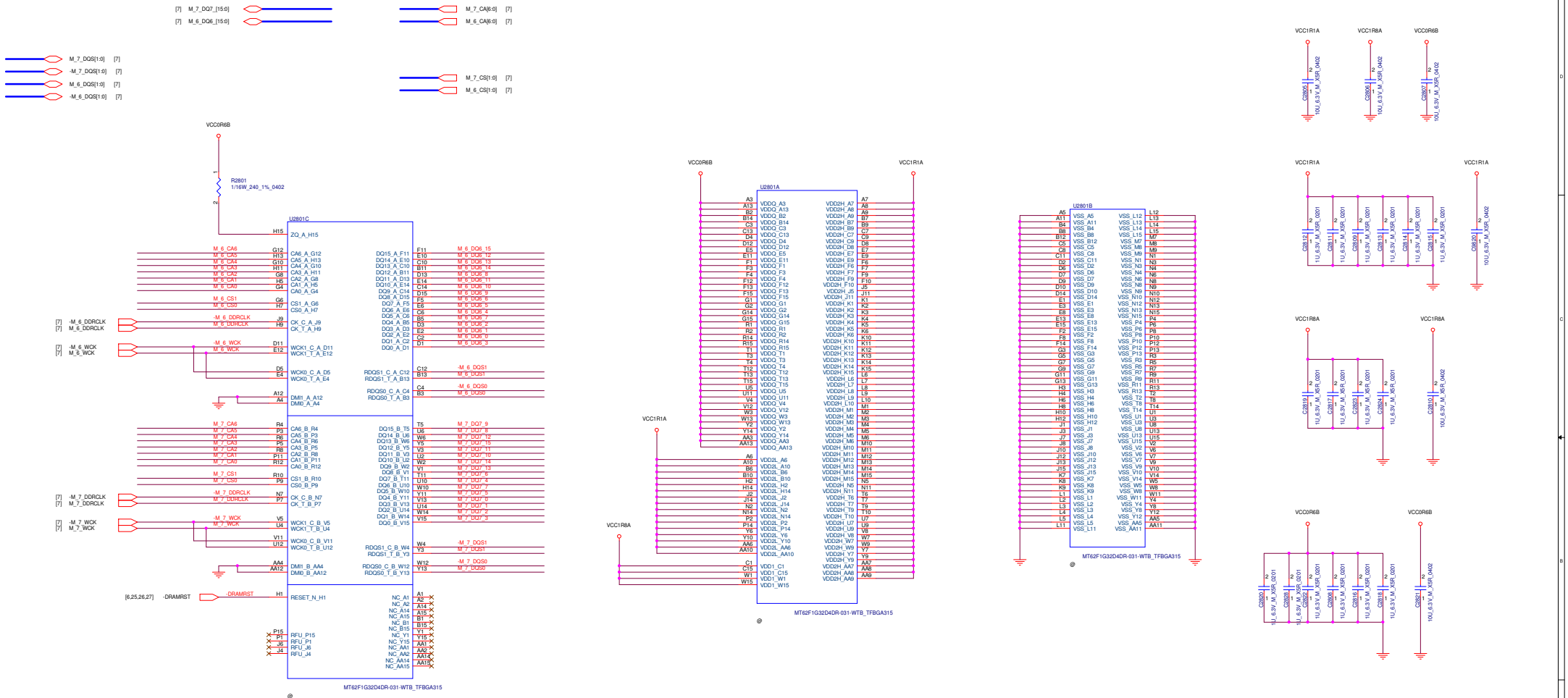

TABLE : LPDDR5 Source

Supplier	Capacity	Supplier's P/N	Package Size		Die	Device Configuration?	Memory
SK Hynix	16Gbit	H9JCNNNBK3MLYR-N6E	12.4 x 15 mm	DDP	8Gb	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	H9JCNNNCP3MLYR-N6E	12.4 x 15 mm	QDP	8Gb	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	H9JCNNNFA5MLYR-N6E	12.4 x 15 mm	ODP	8Gb	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gbit						8GB
	32Gbit	K3LKBKB0BM-MGCP	12.4 x 15 mm	DDP	16Gb	1 Rank x (1Gx16) x 2 Ch	16GB
	64Gbit	K3LKCKC0BM-MGCP	12.4 x 15 mm	QDP	16Gb	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gbit	MT62F512M32D2DR-031	12.4 x 15 mm	DDP	8Gb	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	MT62F1G32D4DR-031	12.4 x 15 mm	QDP	8Gb	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	MT62F2G32D8DR-031	12.4 x 15 mm	ODP	8Gb	2 Rank x (1Gx16) x 2 Ch	32GB

Document Number		LCFC	
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Title	<Title>		
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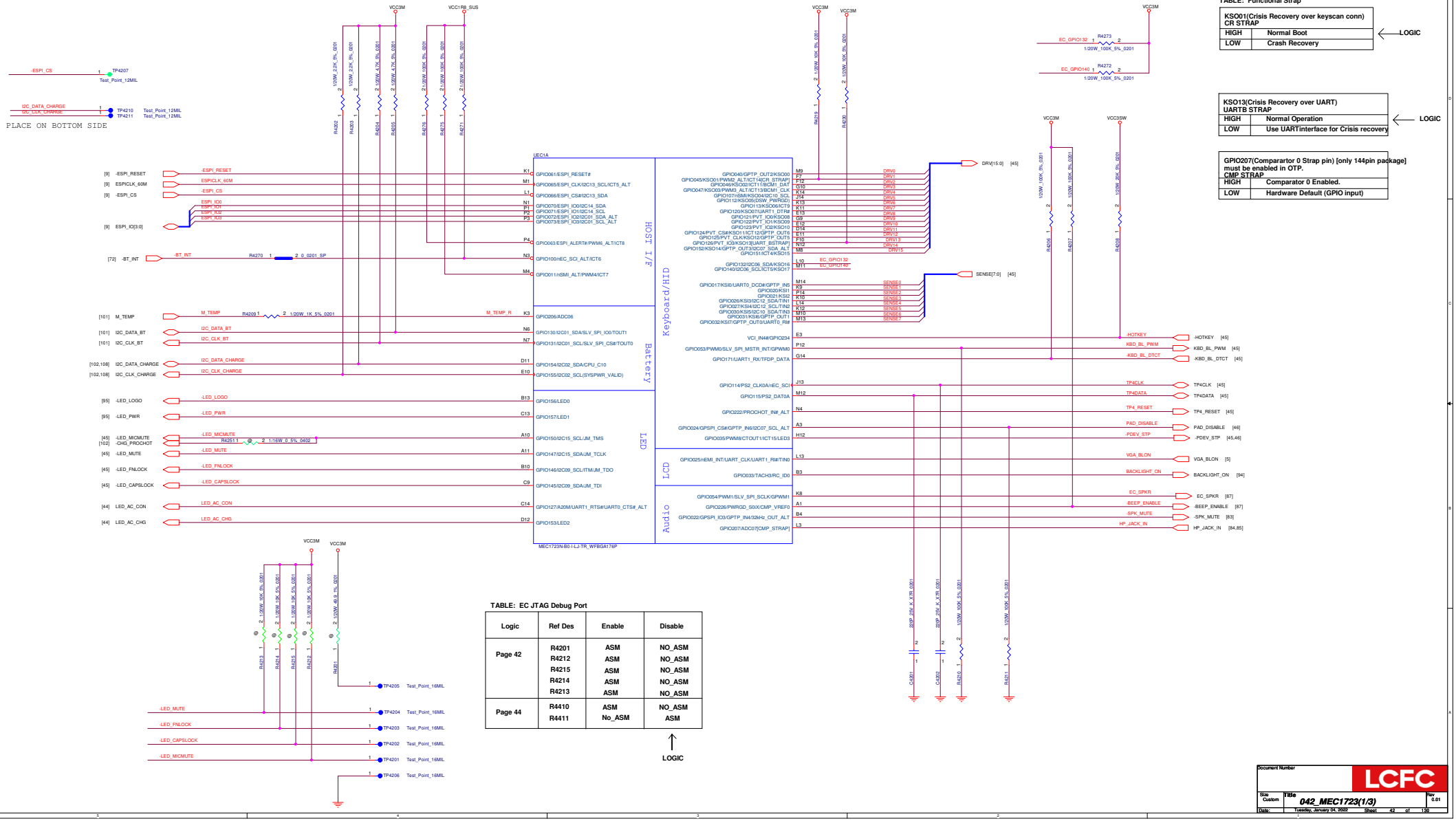

TABLE: Functional Strap

KSO01(Crisis Recovery over keyscan conn) CR STRAP		LOGIC
HIGH	Normal Boot	
LOW	Crash Recovery	

KSO13(Crisis Recovery over UART) UARTB STRAP		LOGIC
HIGH	Normal Operation	
LOW	Use UARTinterface for Crisis recovery	

GPIO207(Compararter 0 Strap pin) [only 144pin package] must be enabled in OTP. CMP STRAP	
HIGH	Comparator 0 Enabled.
LOW	Hardware Default (GPIO input)

TABLE: EC JTAG Debug Port

Logic	Ref Des	Enable	Disable
Page 42	R4201	ASM	NO_ASM
	R4212	ASM	NO_ASM
	R4215	ASM	NO_ASM
	R4214	ASM	NO_ASM
	R4213	ASM	NO_ASM
Page 44	R4410	ASM	NO_ASM
	R4411	No_ASM	ASM

LOGIC

Document Number			LCFC
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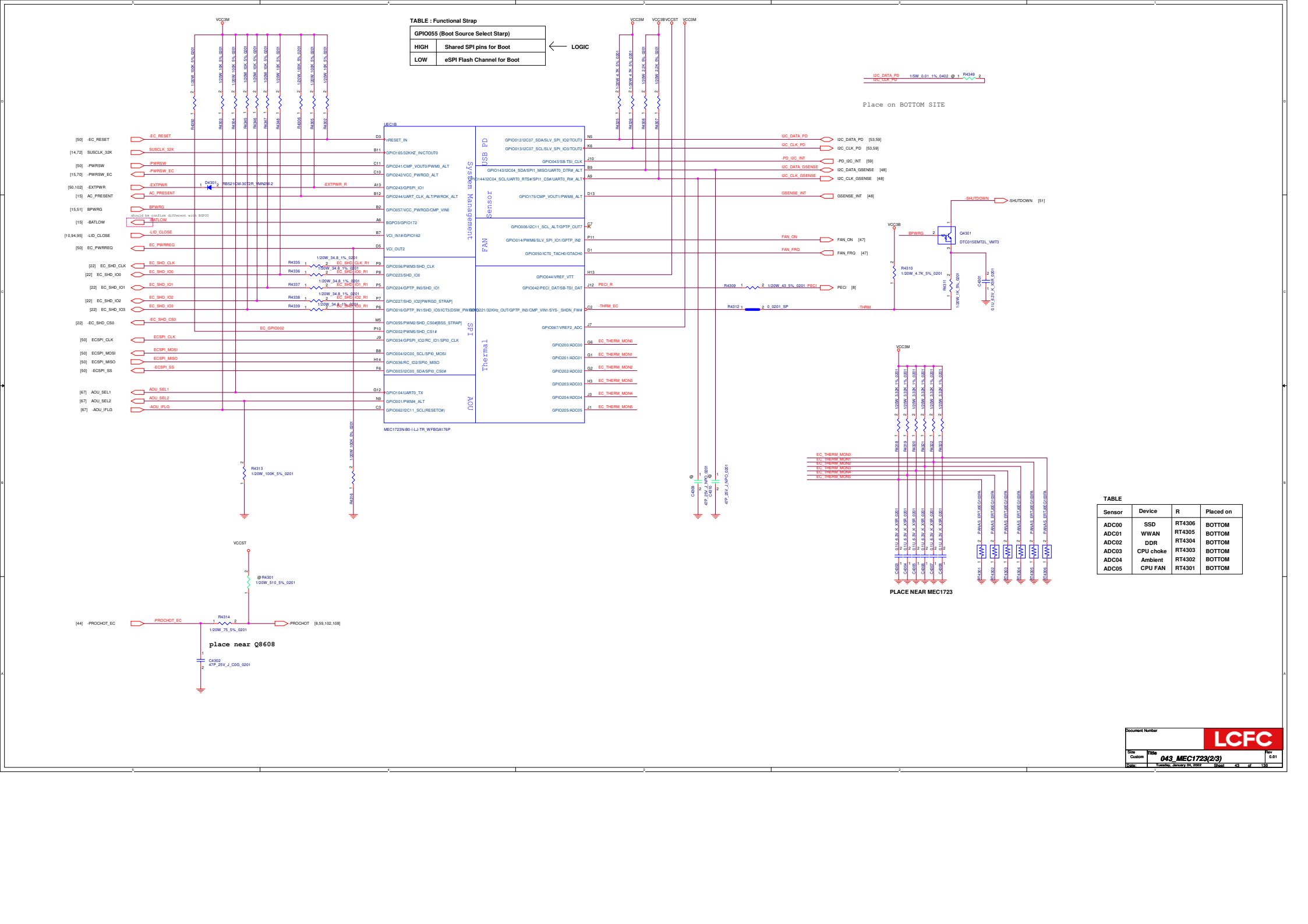
TABLE : Functional Strap
GPIO055 (Boot Source Select Starp)
HIGH Shared SPI pins for Boot
LOW eSPI Flash Channel for Boot
LOGIC
MEC1723N-B0-I-LJ-TR_WFBGA176P
Place on BOTTOM SITE
PLACE NEAR MEC1723
place near Q8608
TABLE
Sensor Device R Placed on
ADC00 SSD RT4306 BOTTOM
ADC01 WWAN RT4305 BOTTOM
ADC02 DDR RT4304 BOTTOM
ADC03 CPU choke RT4303 BOTTOM
ADC04 Ambient RT4302 BOTTOM
ADC05 CPU FAN RT4301 BOTTOM
Document Number
LCFC
Size Custom
Title 043_MEC1723(2/3)
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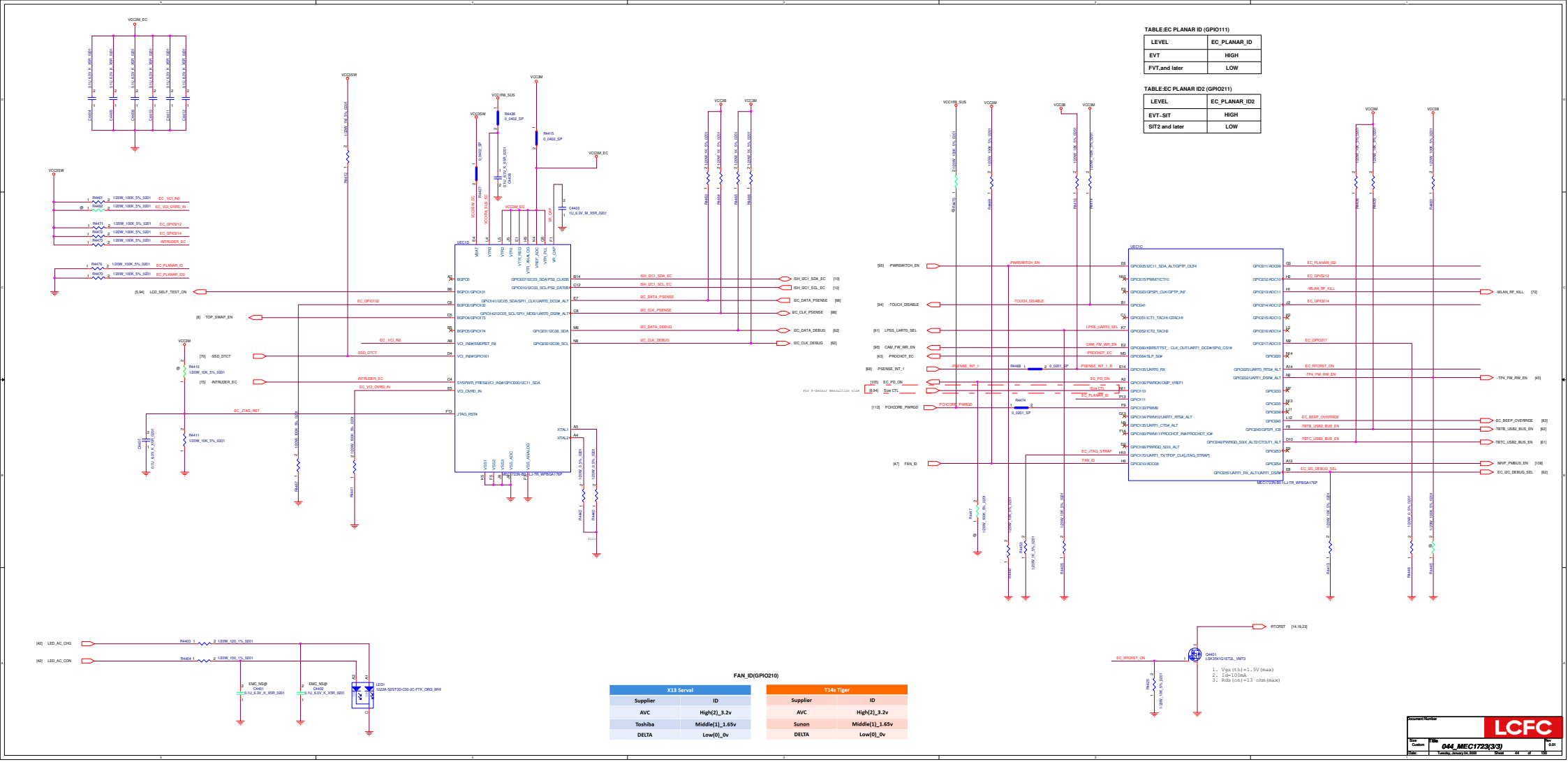

TABLE:EC PLANAR ID (GPIO111)

LEVEL	EC_PLANAR_ID
EVT	HIGH
FVT,and later	LOW

TABLE:EC PLANAR ID2 (GPIO211)

LEVEL	EC_PLANAR_ID2
EVT-SIT	HIGH
SIT2 and later	LOW

FAN_ID(GPIO210)

X13 Serval	
Supplier	ID
AVC	High(2)_3.2v
Toshiba	Middle(1)_1.65v
DELTA	Low(0)_0v

T14s Tiger	
Supplier	ID
AVC	High(2)_3.2v
Sunon	Middle(1)_1.65v
DELTA	Low(0)_0v

1. Vgs(th)=1.5V(max)
2. Id=100mA
3. Rds(on)=13 ohm(max)

Size: Custom	File: 044_MEC1723(3/3)		Rev: 0.01
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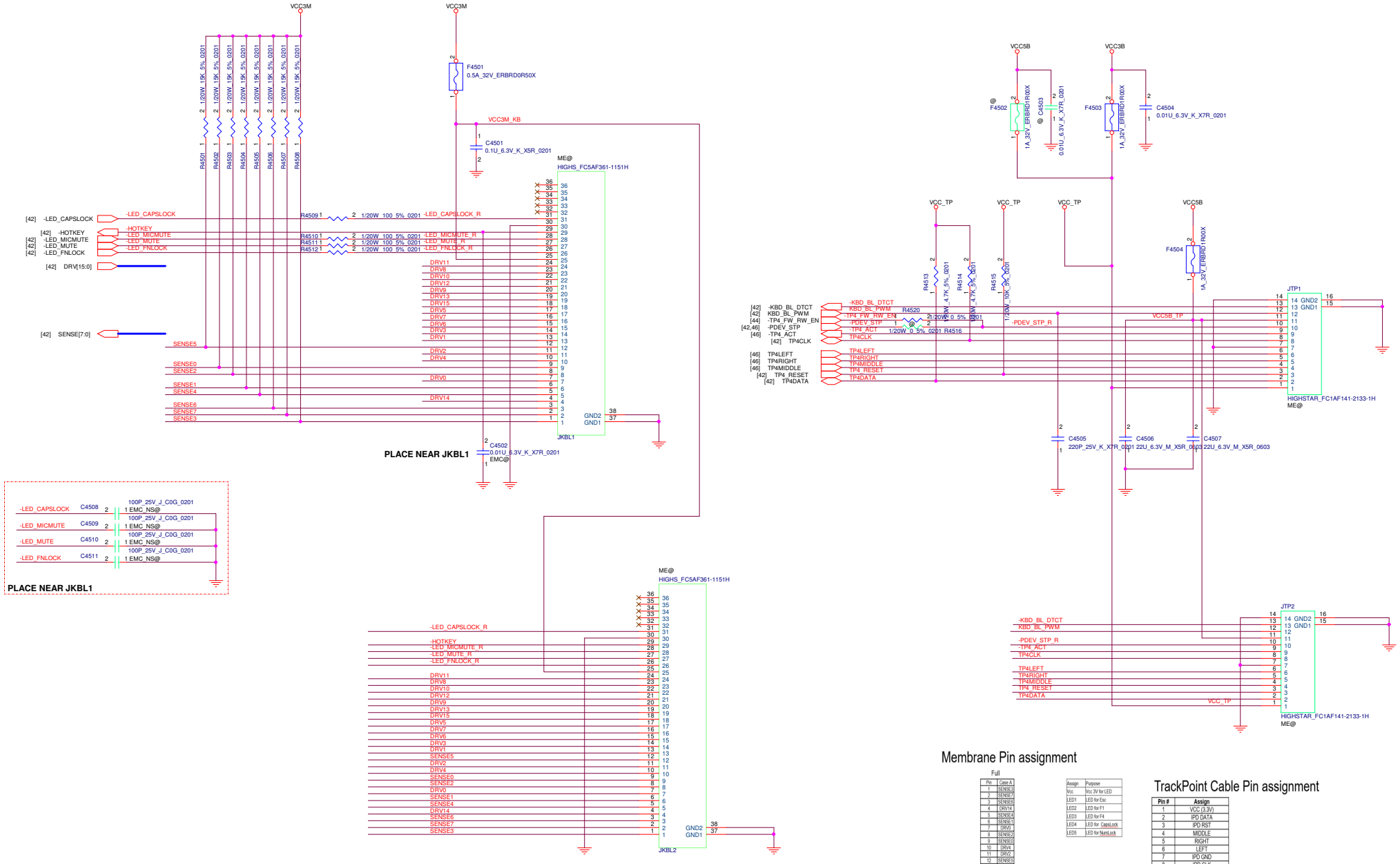

Membrane Pin assignment

Full

Pin	Case A
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV0
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	HOTKEY
30	GND
31	LED4
32	NC
33	NC
34	NC
35	NC
36	NC

Assign	Purpose
Vcc	Vcc 3V for LED
LED1	LED for Esc
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLock
LED5	LED for NumLock

TrackPoint Cable Pin assignment

Pin #	Assign
1	VCC (3.3V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	-TP4_ACT
10	-TP4_FW_RW_EN
11	LED VCC5 (5V)
12	LED PWM
13	Backlight detection
14	LED GND

Matrix Mapping and Me

Sense (S1 ~ S8)

Drive (D1 ~ D16)

	SEN S1	SEN S2	SEN S3	SEN S4	SEN S5	SEN S6	SEN S7	SEN S8	HOT KEY
DRV0	1	2	17	16	31	110	46	131	
DRV1	112	3	18	30	32	45	47		
DRV2	113	4	19	114	33	115	48		
DRV3	6	5	20	21	34	35	49	50	
DRV4	7	8	23	22	37	36	52	51	
DRV5	13	9	24	28	38	117	53	56	
DRV6	119	10	25	118	39	132	54	133	
DRV7	12	11	26	27	40	41	42	55	
DRV8	120	121	14	15	29	116	43	61	
DRV9	75	123	104	VVs				69	
DRV10	76	122	E23	E22	E24	E21		64	
DRV11	85	86	130	129	App		INS	INF	
DRV12	80	81	128	127		83	125	79	
DRV13		124	125			66		62	
DRV14				44		65	67	63	
DRV15	58						64		
DRV16	105	96	100	95	91	90	101	106	
DRV17	93	103	102	97	98	92	108	99	
GND									Fn

This matrix has some unnecessary mappings (e.g. 125, E2#, etc.) due universal use purpose.

JKBL1(36Pin) & JTP1: Serval2_X13 => Top side
JKBL2(36Pin) & JTP2: Phoenix_T14s => Bot side (CPU)
EVT

Lenovo		
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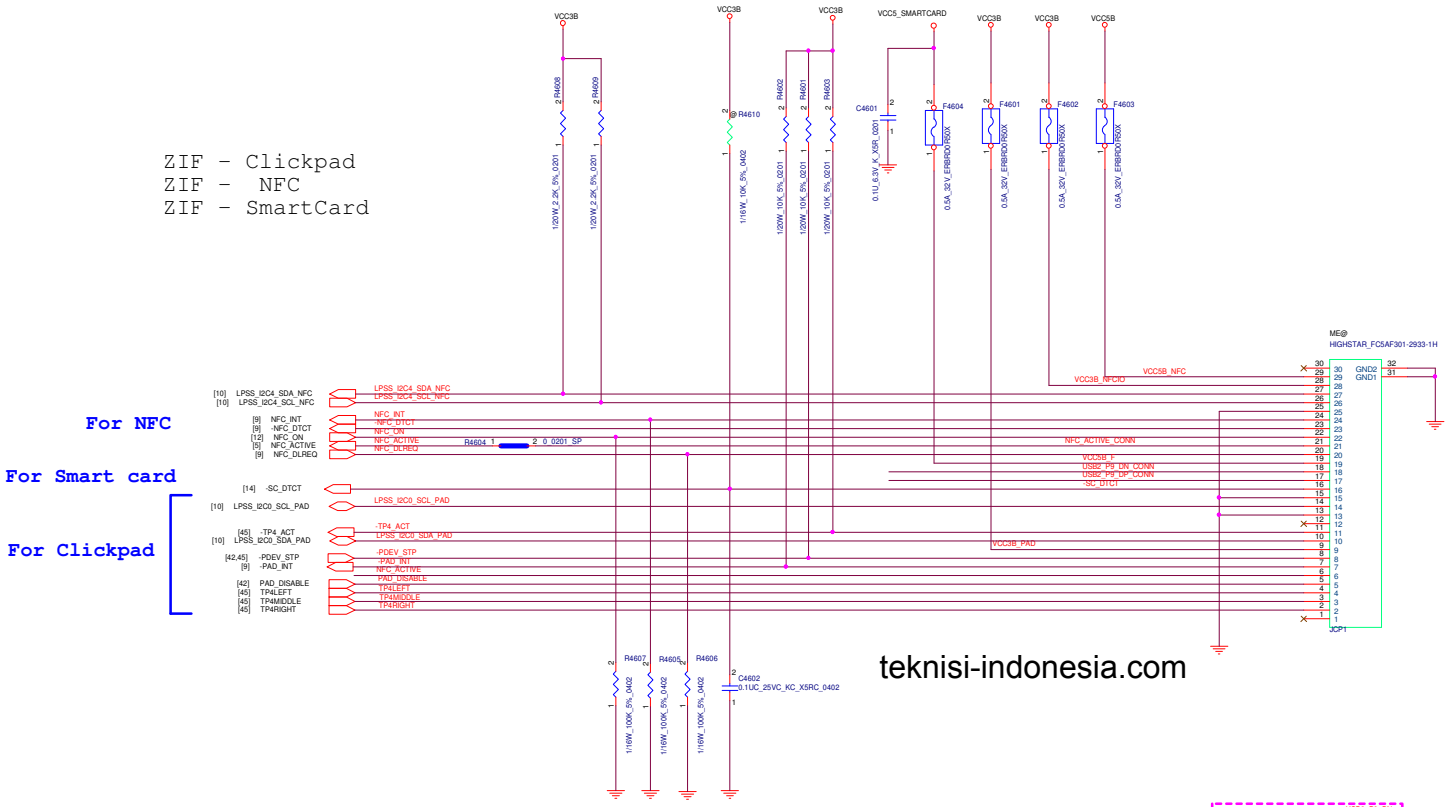
ZIF - Clickpad
ZIF - NFC
ZIF - SmartCard



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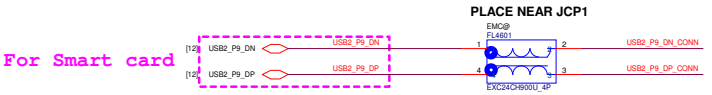

For NFC 3/24 OK

Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C _SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

For Clickpad 03/24 OK

Original pin assign

Name	Pin#	Type	Function
GND	1	Power	Signal Ground
I2C_CLK	2	IN/OUT	I2C Clock to System I2C I/F on CPU/PCH
IPD_GND	3	IN	TrackPoint ground
NC	4		
-TP4_ACT	5	IN	TrackPoint Activity status. Please refer to "4.2.8"
I2C_DAT	6	IN/OUT	I2C Data to System I2C I/F on CPU/PCH
VDD	7	Power	Supply power from system. Power is not supplied when system is in S3, S4, S5 and G5 state. (Refer to electrical requirement)
- PDEV_STP	8	IN	This signal is used to disable to report button status and finger status to system when system LCD lid is closed or is in Tent /Stand /Tablet modes (Yoga case). Please refer to "4.2.5-PDEV_STP"
-I2C_INT	9	OUT	Interrupt for I2C communication
NFC_Active	10	IN	This signal should use if NFC Antenna is implemented under touch pad PCBA. This signal should be NC or not be used in touch pad PCBA if NFC antenna is not implemented under touch pad PCBA. Please refer to "4.2.6 NFC_Active"
PAD_DISABLE	11	IN	This signal is used to disable touch pad. Please refer to "4.2.4 PAD_DISABLE".
TP4LEFT	12	IN	TrackPoint button signal
TP4MIDDLE	13	IN	TrackPoint button signal
TP4RIGHT	14	IN	TrackPoint button signal

For Smart card 3/24 OK

PIN ASSIGNMENT	
PIN #	DESCRIPTION
#1	VCC +5V
#2	USB D–
#3	USB D+
#4	GND
#5	NC
#6	GND

Lenovo

Project Name : T14s Gen2	Title : TOUCH PAD/Smart card/NFC
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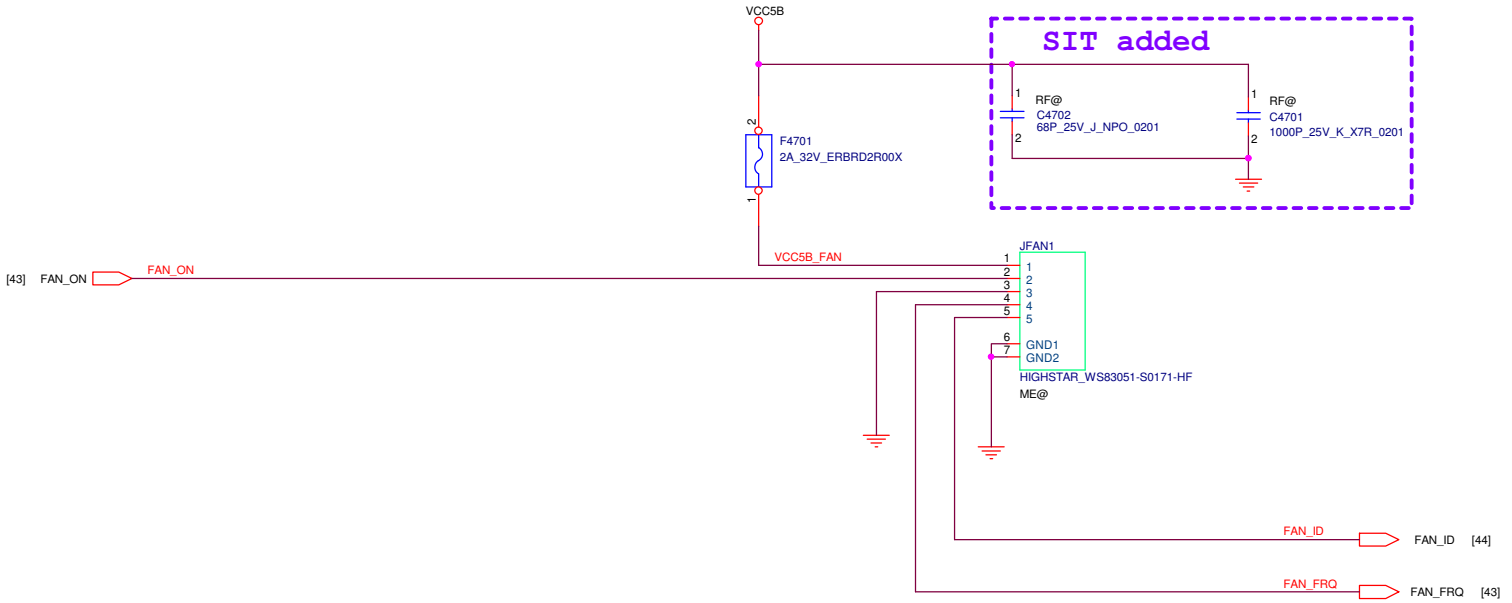

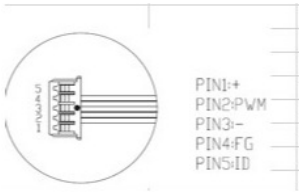

Pin No.	Signal	Note	Color
1	VCC	+5V	Black
2	PWM	PWM	Black
3	GND	–	Black
4	FG	2 Pulses	Black
5	ID	Fan ID	Black
--	–		

Security Classification	LC Future Center Secret Data		
Issued Date	2018/01/12	Deciphered Date	2018/01/12

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Title: **FAN CONNECTOR**

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TABLE : U4801

P/N	ADDR_SEL	Address
LIS2DWLTR	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX022-1020	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)
BMA422	H L	32h (W) & 33h (R) 30h (W) & 31h (R)

ST and Bosch I2C address is same but can be identified by Chip_ID

TABLE of G-Sensor (U4801)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00
BOSCH	BMA422	SA0000C1V00

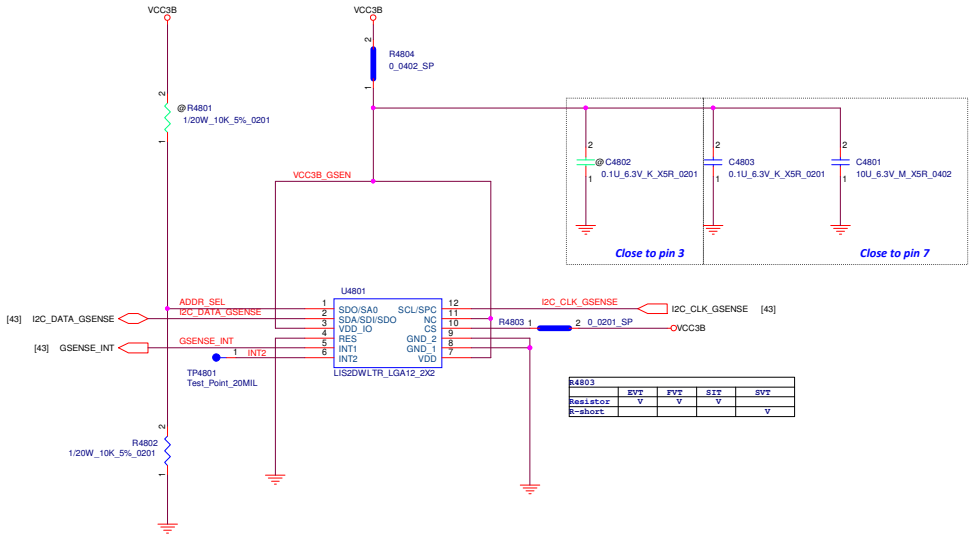
Table 2. Pin description

Pin#	Name	Function
1	SDO SA0	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)
2	SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
3	Vdd_IO	Power supply for I/O pins
4	RES	Connect to GND
5	INT1	Interrupt pin 1
6	INT2	Interrupt pin 2
7	Vdd	Power supply
8	GND	0 V supply
9	GND	0 V supply
10	CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
11	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.
12	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)

TABLE : G-Sensor Power

HDD Support	VCC3M
SSD Only	VCC3B

EC Control



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Project Name : T14s Gen2	Title : APS G-SENSOR
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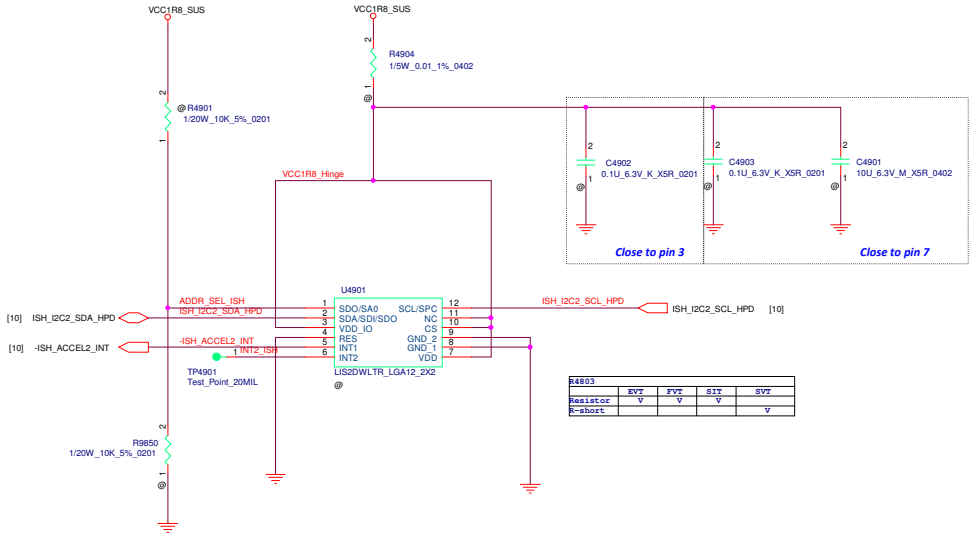
ISH_Control

TABLE : U4901

P/N	ADDR_SEL	Address
LIS2DWLTR	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX022-1020	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)
BMA422	H L	32h (W) & 33h (R) 30h (W) & 31h (R)



	Project Name :	Title :
Lenovo	T14s Gen2	ISH_Control_G-Sensor
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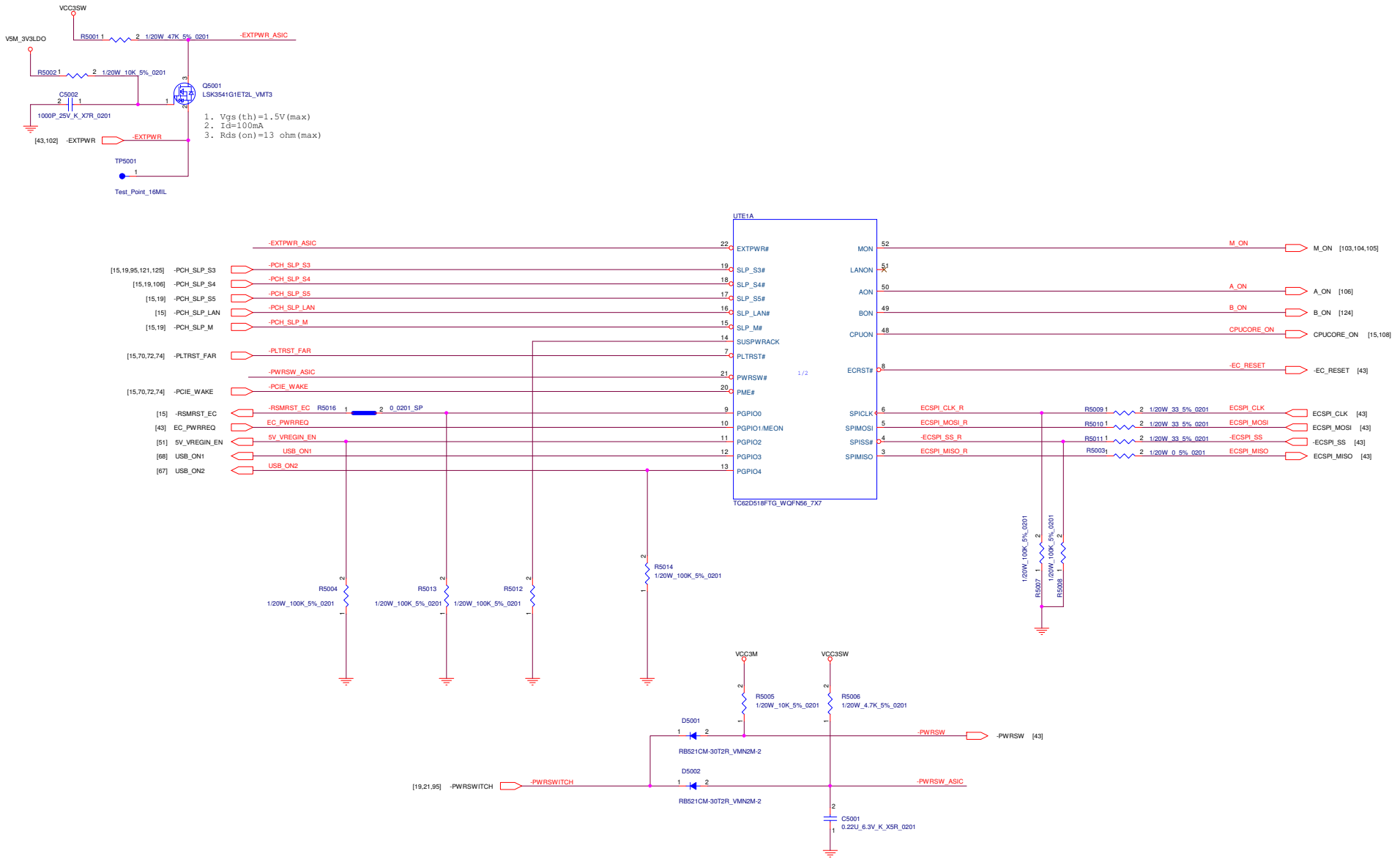

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Table D5102,D5106

ROHM:
Toshiba: 1SS417

Q5103
1. Vgs(th)=-1.7V(max)
2. Id=-100mA
3. Rds(on)=32 ohm(max)

R413, R422 : Need Anti-surge Chip Resistors

Total capacitance of VCC3SW MLCCs must be less than 4.7uF.

Q5101
1. Vgs(th)=1.5V(max)
2. Id=100mA
3. Rds(on)=13 ohm(max)

Q5102
1. Vgs(th)=1.5V(max)
2. Id=100mA
3. Rds(on)=13 ohm(max)

ID	Target
RT5101	TBTB_VBUS20_F to VINT20_IN FET (Q6501)
RT5102	TBTC_VBUS20_F to VINT20_IN FET (Q6505)
RT5103	VCCCPUCORE DrMOS (PL0906)
RT5104	VCCCPUCORE DrMOS (PL0901)
RT5105	VCCPCHCORE VR IC (PL1201)
RT5106	CPU Die (UCPU1)
RT5107	VCCGT DrMOS (PL1101)
RT5108	VCCGT DrMOS (PL1104)
RT5109	VCC1R1A VR IC (PU0601)
RT5110	Battery Charger BUCK Dual FET (PQ0201)
RT5111	Battery Charger BOOST Dual FET (PQ0202)
RT5112	Battery Charger BATDRV FET (PQ0203)
RT5113	MBAT_PWR15 to BAT_PWR15 FET (PQ0101)

Document Number: LCFC

Size: Custom | Title: 051_THINK ENGINE-3(2/2) | Rev: 0.01

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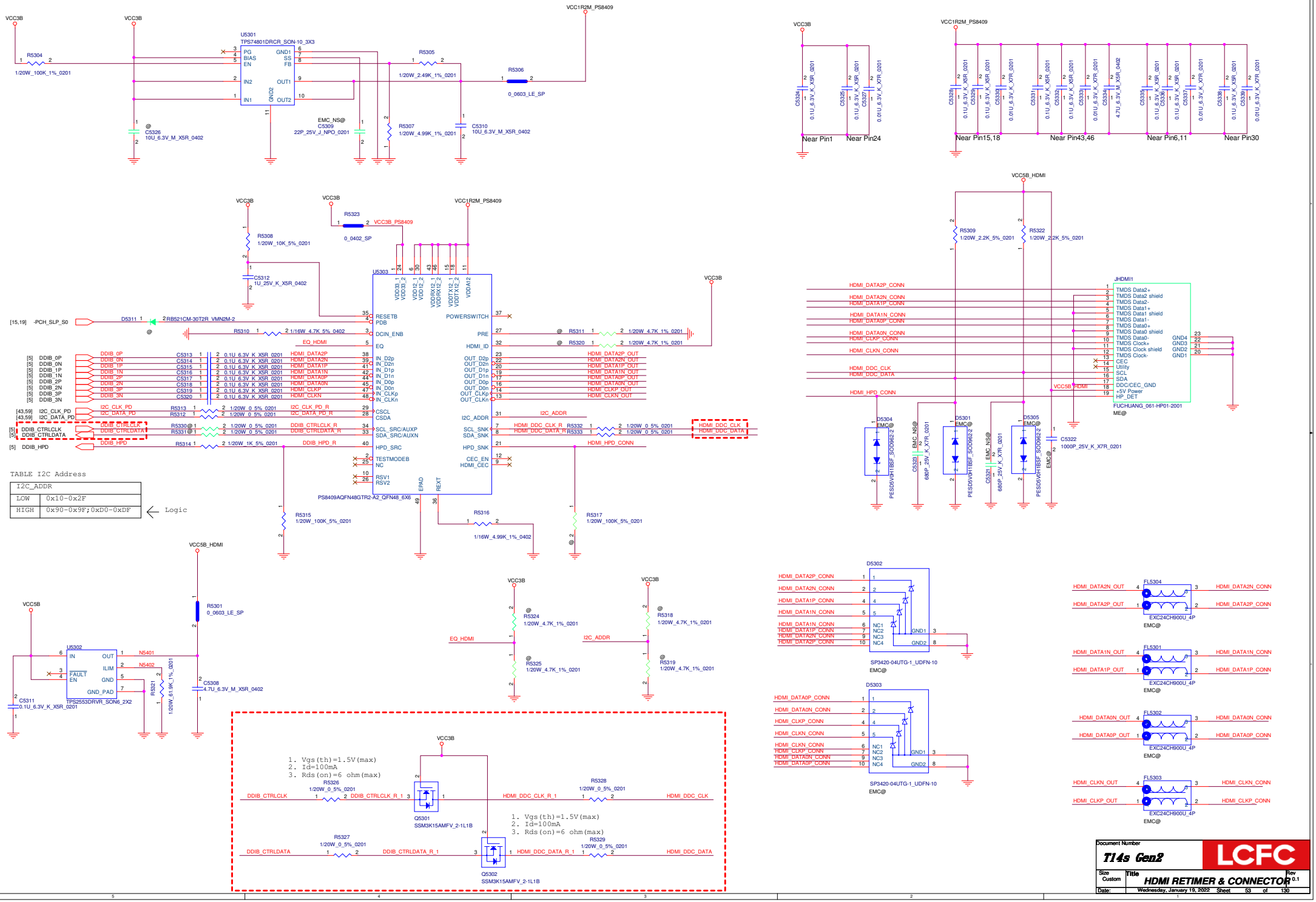
VCC3B
VCC1R2M_PS8409
U5301
TPS74801DRCR_SON-10_3X3
R5304
1/20W_100K_1%_0201
R5305
1/20W_2.49K_1%_0201
R5306
0_0603_LE_SP
R5307
1/20W_4.99K_1%_0201
C5310
10U_6.3V_M_X5R_0402
C5326
10U_6.3V_M_X5R_0402
EMC_NS@
C5309
22P_25V_J_NPO_0201
Near Pin1
Near Pin24
Near Pin15,18
Near Pin43,46
Near Pin6,11
Near Pin30
VCC5B_HDMI
JHDMI1
FUCHUANG_061-HP01-2001
ME@
U5303
PS8409AQFN48GTR2-A2_QFN48_6X6
POWERSWITCH
HDMI_ID
I2C_ADDR
TABLE I2C Address
I2C_ADDR
LOW 0x10~0x2F
HIGH 0x90~0x9F;0xD0~0xDF
Logic
U5302
TPS2553DRVR_SON6_2X2
VCC5B
1. Vgs(th)=1.5V(max)
2. Id=100mA
3. Rds(on)=6 ohm(max)
Q5301
SSM3K15AMFV_2-1L1B
Q5302
SSM3K15AMFV_2-1L1B
SP3420-04UTG-1_UDFN-10
EXC24CH900U_4P
EMC@
Document Number
T14s Gen2
LCFC
Size Custom
Title
HDMI RETIMER & CONNECTOR
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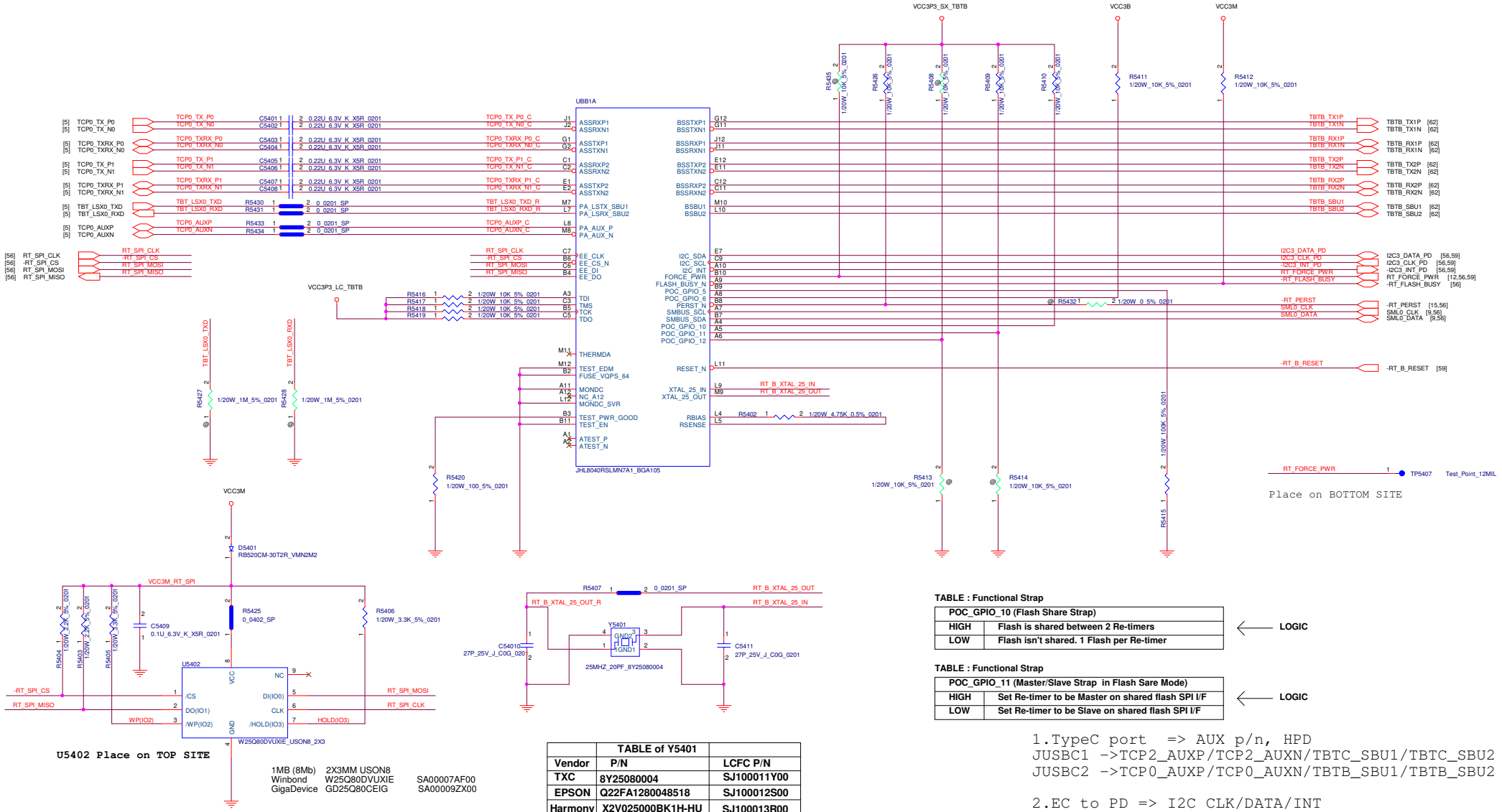


TABLE : Functional Strap

POC_GPIO_10 (Flash Share Strap)		
HIGH	Flash is shared between 2 Re-timers	← LOGIC
LOW	Flash isn't shared. 1 Flash per Re-timer	

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)		
HIGH	Set Re-timer to be Master on shared flash SPI I/F	← LOGIC
LOW	Set Re-timer to be Slave on shared flash SPI I/F	

TABLE of Y5401		
Vendor	P/N	LCFC P/N
TXC	8Y25080004	SJ100011Y00
EPSON	Q22FA1280048518	SJ100012S00
Harmony	X2V025000BK1H-HU	SJ100013R00

1MB (8Mb) 2X3MM USON8
Winbond W25Q80DVUXIE SA00007AF00
GigaDevice GD25Q80CEIG SA00009ZX00

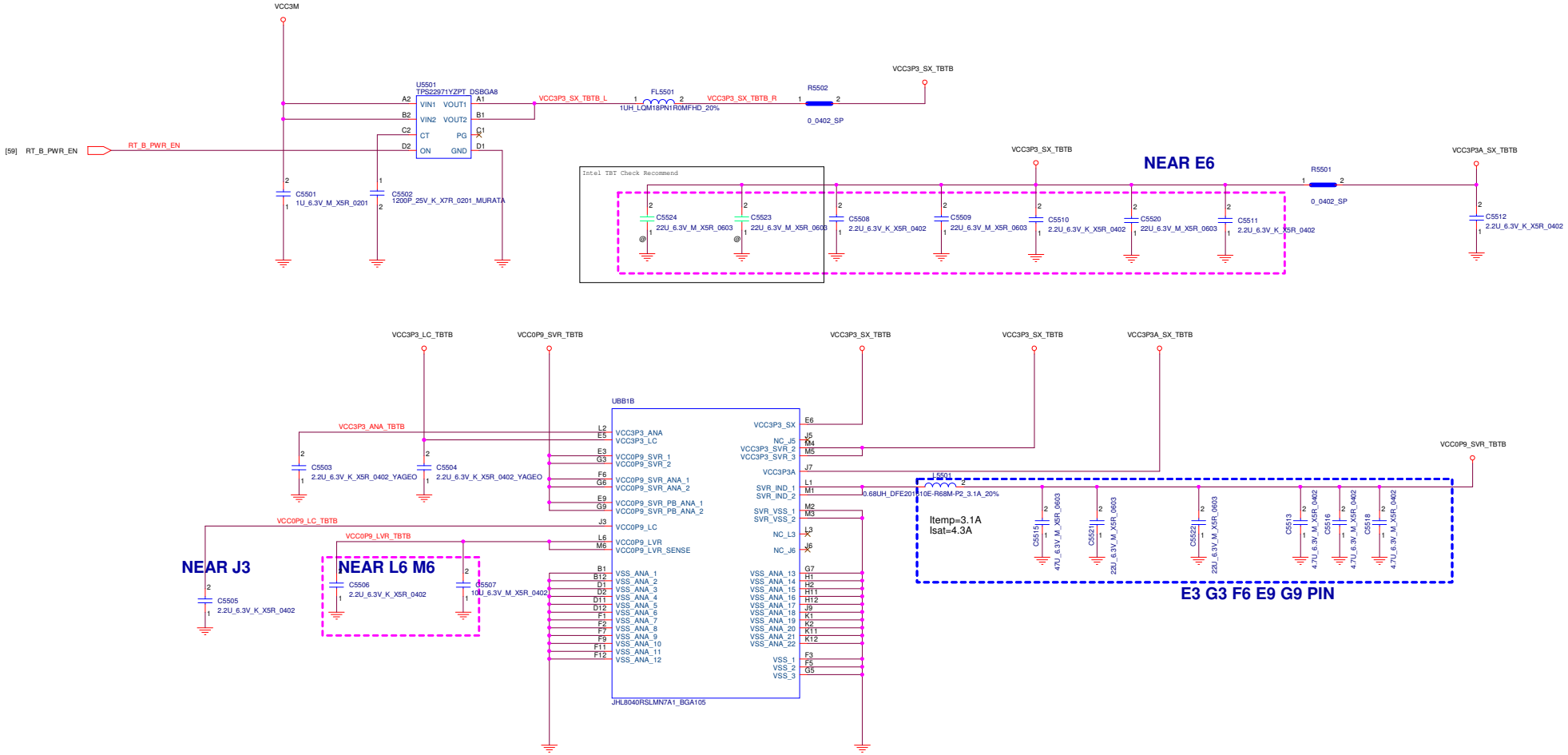
1.TypeC port => AUX p/n, HPD
JUSBC1 ->TCP2_AUXP/TCP2_AUXN/TBTC_SBU1/TBTC_SBU2
JUSBC2 ->TCP0_AUXP/TCP0_AUXN/TBTB_SBU1/TBTB_SBU2

2.EC to PD => I2C CLK/DATA/INT
I2C_DATA_PD/I2C_CLK_PD/-PD_I2C_INT

3.PCH(PMC(TBT)) to PD => I2C CLK/DATA/INT
SML1_CLK/SML1_DATA/-PMC_ALERT

4.PD to BB => I2C CLK/DATA
I2C3_CLK_PD/I2C3_DATA_PD/-I2C3_INT_PD

Document Number	LCFC	
Size: Custom	Title: 054_THUNDERBOLT RETIMER B (1/2)	Rev: B01
Date: Tuesday, January 04, 2022	Sheet 54 of 130	



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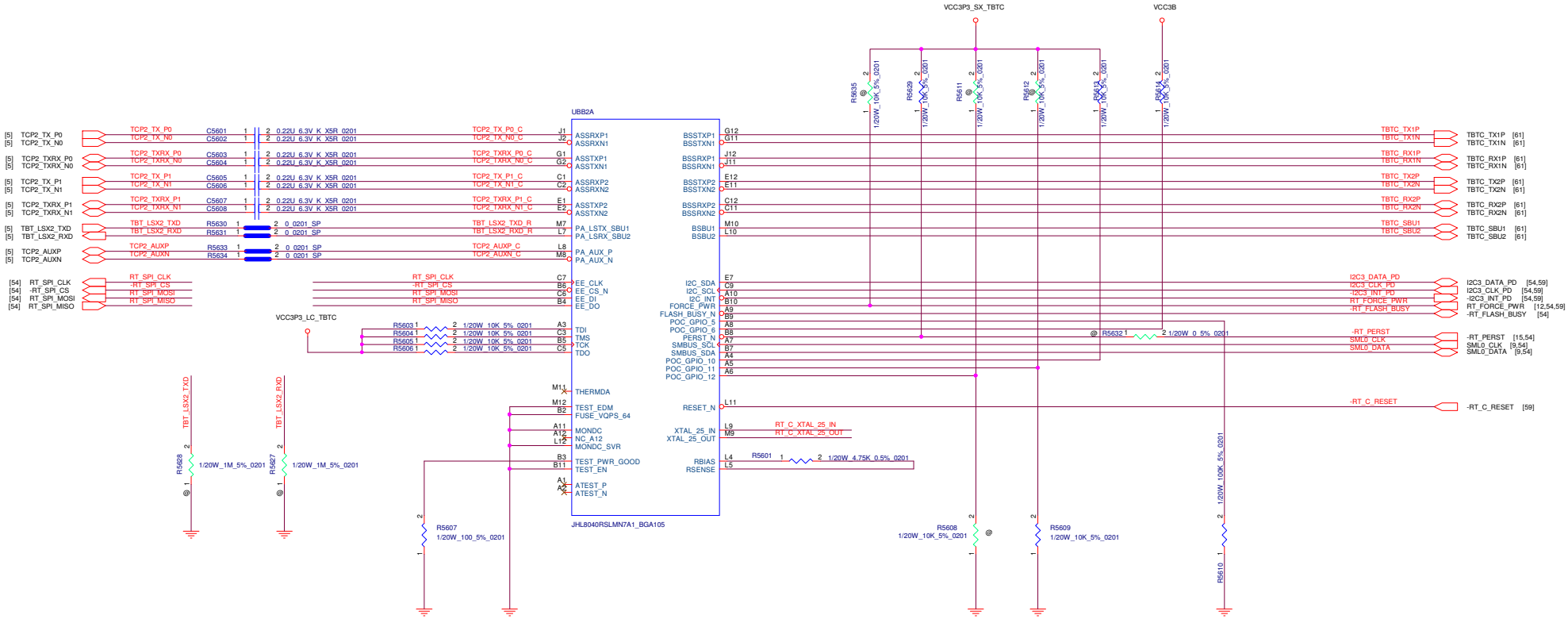
Size: Custom	Title: 055_THUNDERBOLT RETIMER B (2/2)		
Date: Tuesday, January 04, 2022	Sheet 55 of 130		



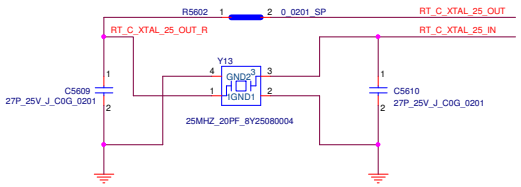


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TABLE : Functional Strap

POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

← LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

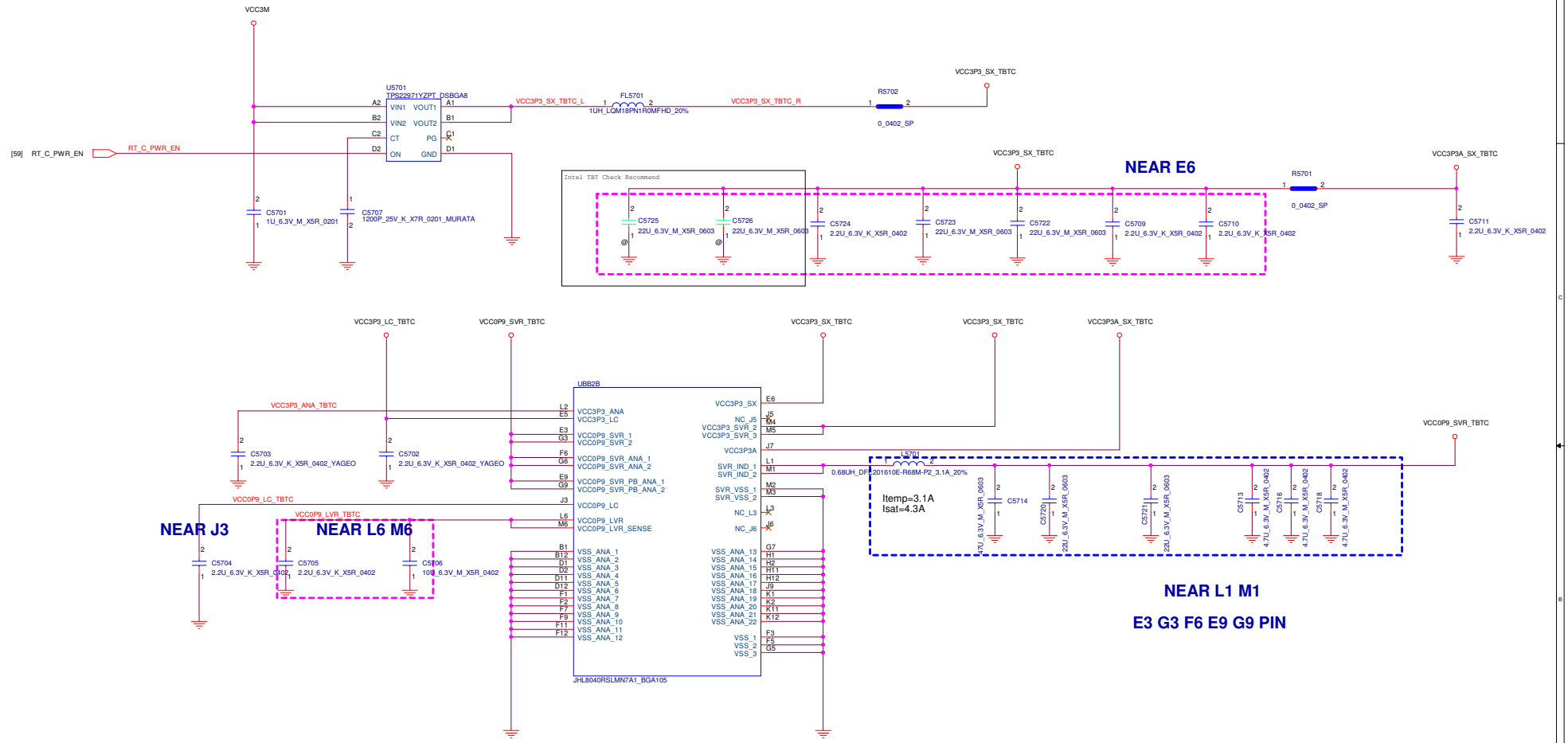
← LOGIC

Table 8. Miscellaneous Signal and Pin Information

Signal	Pin Number	Type	Power domain	Internal PU / PD	Fail-Safe	Description
I2C_SCL	C9	I/O	POC		Yes	I2C bus clock line
I2C_SDA	E7	I/O	POC		Yes	I2C bus data line
I2C_INT	A10	OD	POC		Yes	I2C bus interrupt
FORCE_PWR	B10	I/O	POC		Yes	GPIO Debug
FLASH_BUSY_N	A9	I/O	POC		Yes	GPIO Flash sharing control
POC_GPIO_5	B9	I/O	POC		Yes	GPIO
POC_GPIO_6	A8	I/O	POC		Yes	GPIO (should be connected to system S0 rail)
PERST_N	B8	I/O	POC		Yes	System PERST
SMBUS_SCL	A7	I/O	POC		Yes	SMBus clock
SMBUS_SDA	B7	I/O	POC		Yes	SMBus data
POC_GPIO_10	A4	I/O	POC	PU	Yes	GPIO (Used as Flash share strap)
POC_GPIO_11	A5	I/O	POC	PU	Yes	GPIO (Master-1/Slave-0 strap in Flash share mode)
POC_GPIO_12	A6	I/O	POC	PU	Yes	GPIO
RESET_N	L11	I/O	POC			Main power reset signal
RBIAS	L4	A-in				External resistor for current biasing Resistor value 4.75KOhm +/- 0.5%
RSENSE	L5	A-in				Shares same external resistor as RBIAS
TEST_EDM	M12	In			Yes	Testability signal, connect to GND
THERMDA	M11	A-out	LC			Thermal Diode pin (anode)
NC_L3	L3					

TABLE of Y13		
Vendor	P/N	LCFC P/N
TXC	8Y25080004	SJ100011Y00
EPSON	Q22FA1280048518	SJ100012S00
Harmony	X2V025000BK1H-HU	SJ100013R00

Document Number	LCFC	Rev
Size: Custom	Title: 056_THUNDERBOLT RETIMER C (1/2)	
Date: Tuesday, January 04, 2022	Sheet 56 of 130	



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Size: Custom	Title: 057_THUNDERBOLT RETIMER C (2/2)	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 57 of 130	

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Project Name : T14s Gen2	Title : BLANK
Size : C	Document Number :
Rev : 0.1	
Date: Tuesday, January 04, 2022	Sheet : 58 of 130

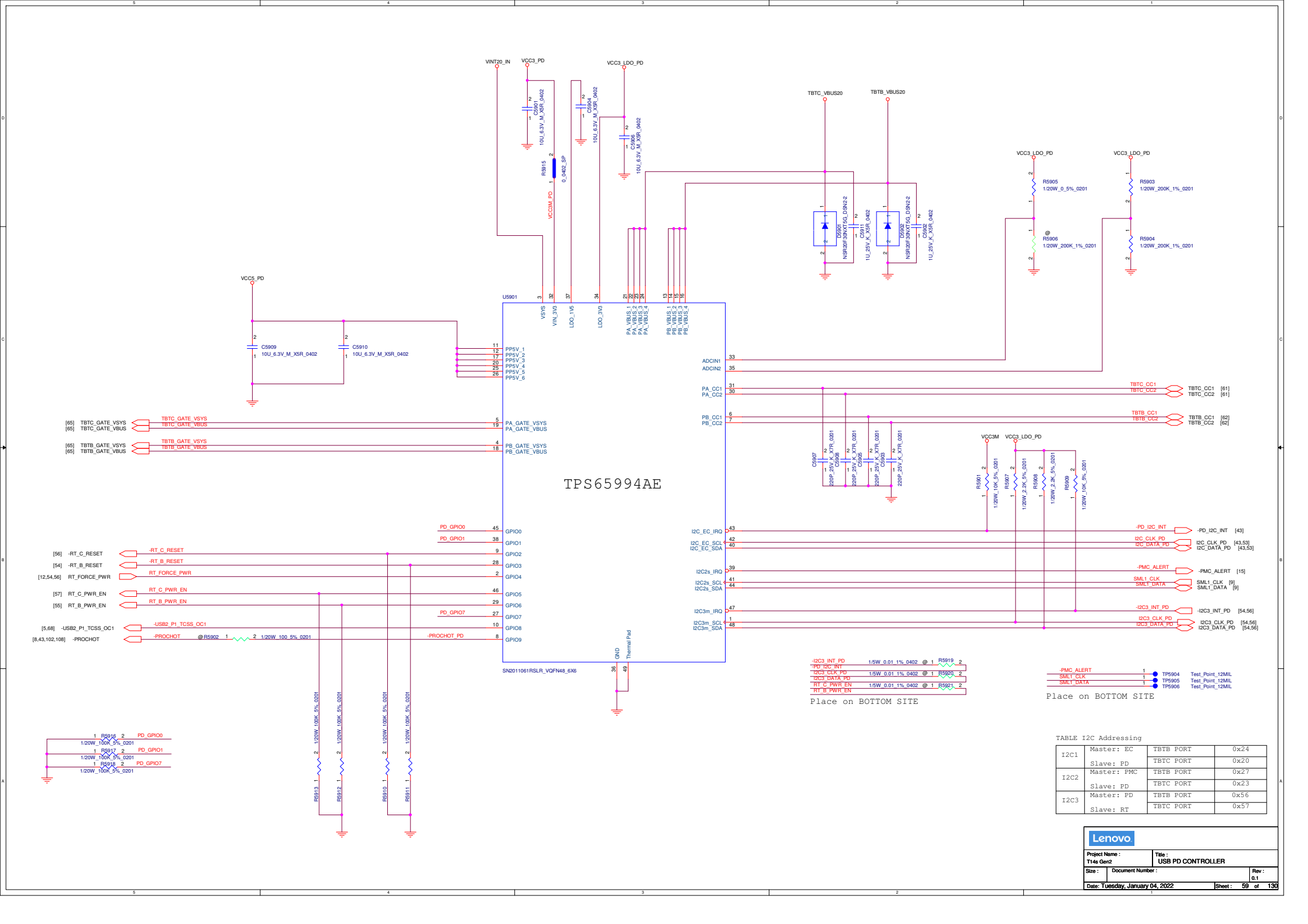

TABLE I2C Addressing

I2C1	Master: EC	TBTB PORT	0x24
	Slave: PD	TBTC PORT	0x20
I2C2	Master: PMC	TBTB PORT	0x27
	Slave: PD	TBTC PORT	0x23
I2C3	Master: PD	TBTB PORT	0x56
	Slave: RT	TBTC PORT	0x57

Lenovo

Project Name : T14s Gen2	Title : USB PD CONTROLLER
Size :	Document Number : Rev : 0.1
Date: Tuesday, January 04, 2022	Sheet : 59 of 130

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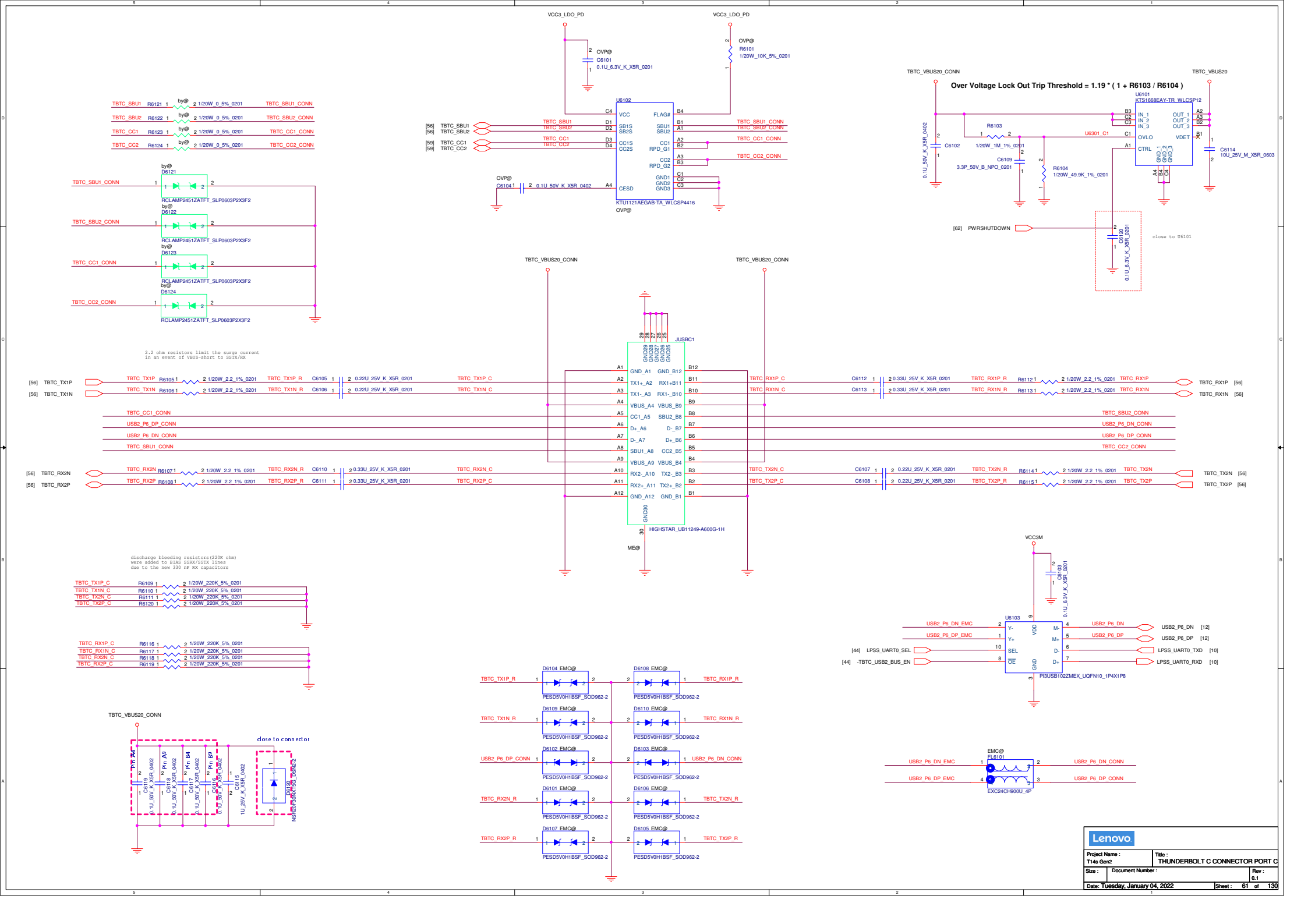
Title	<Title>		
Size	Document Number		Rev
Custom	T14s Gen2		0.1
Date:	Tuesday, January 04, 2022	Sheet 60 of 130	


VCC3_LDO_PD
VCC3_LDO_PD
OVP@
C6101
0.1U_6.3V_K_X5R_0201
OVP@
R6101
1/20W_10K_5%_0201
U6102
KTU1121AEGAB-TA_WLCSP4416
OVP@
C6104
0.1U_50V_K_X5R_0402
TBTC_SBU1
TBTC_SBU2
TBTC_CC1
TBTC_CC2
TBTC_SBU1_CONN
TBTC_SBU2_CONN
TBTC_CC1_CONN
TBTC_CC2_CONN
TBTC_VBUS20_CONN
TBTC_VBUS20
Over Voltage Lock Out Trip Threshold = 1.19 * (1 + R6103 / R6104)
U6101
KTS1668EAY-TR_WLCSP12
R6103
1/20W_1M_1%_0201
R6104
1/20W_49.9K_1%_0201
C6109
3.3P_50V_B_NPO_0201
C6102
0.1U_50V_K_X5R_0402
C6114
10U_25V_M_X5R_0603
C6120
0.1U_6.3V_K_X5R_0201
close to U6101
[62] PWRSHUTDOWN
TBTC_SBU1_CONN
TBTC_SBU2_CONN
TBTC_CC1_CONN
TBTC_CC2_CONN
D6121
D6122
D6123
D6124
RCLAMP2451ZATFT_SLP0603P2X3F2
2.2 ohm resistors limit the surge current
in an event of VBUS-short to SBTX/RX
TBTC_VBUS20_CONN
TBTC_VBUS20_CONN
JUSBC1
HIGHSTAR_UB11249-A600G-1H
ME@
[56] TBTC_TX1P
[56] TBTC_TX1N
[56] TBTC_RX2N
[56] TBTC_RX2P
TBTC_RX1P [56]
TBTC_RX1N [56]
TBTC_TX2N [56]
TBTC_TX2P [56]
R6105
R6106
R6107
R6108
R6112
R6113
R6114
R6115
C6105
C6106
C6110
C6111
C6112
C6113
C6107
C6108
0.22U_25V_K_X5R_0201
0.33U_25V_K_X5R_0201
2 1/20W_2.2_1%_0201
TBTC_CC1_CONN
USB2_P6_DP_CONN
USB2_P6_DN_CONN
TBTC_SBU1_CONN
TBTC_SBU2_CONN
USB2_P6_DN_CONN
USB2_P6_DP_CONN
TBTC_CC2_CONN
discharge bleeding resistors(220K ohm)
were added to BIAS SSRX/SSTX lines
due to the new 330 nF RX capacitors
R6109
R6110
R6111
R6120
R6116
R6117
R6118
R6119
2 1/20W_220K_5%_0201
VCC3M
U6103
PI3USB102ZMEX_UQFN10_1P4X1P8
USB2_P6_DN_EMC
USB2_P6_DP_EMC
USB2_P6_DN [12]
USB2_P6_DP [12]
[44] LPSS_UART0_SEL
[44] -TBTC_USB2_BUS_EN
LPSS_UART0_TXD [10]
LPSS_UART0_RXD [10]
TBTC_VBUS20_CONN
close to connector
Pin A4
Pin A9
Pin B4
Pin B9
C6119
C6118
C6117
C6116
C6115
0.1U_50V_K_X5R_0402
1U_25V_K_X5R_0402
PESD5V0H1BSF_SOD962-2
D6104 EMC@
D6108 EMC@
D6109 EMC@
D6110 EMC@
D6102 EMC@
D6103 EMC@
D6101 EMC@
D6106 EMC@
D6107 EMC@
D6105 EMC@
TBTC_TX1P_R
TBTC_RX1P_R
TBTC_TX1N_R
TBTC_RX1N_R
TBTC_RX2N_R
TBTC_TX2N_R
TBTC_RX2P_R
TBTC_TX2P_R
USB2_P6_DP_CONN
USB2_P6_DN_CONN
EMC@
FL6101
EXC24CH900U_4P
USB2_P6_DN_CONN
USB2_P6_DP_CONN
Lenovo
Project Name :
T14s Gen2
Title :
THUNDERBOLT C CONNECTOR PORT C
Size :
Document Number :
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0.1
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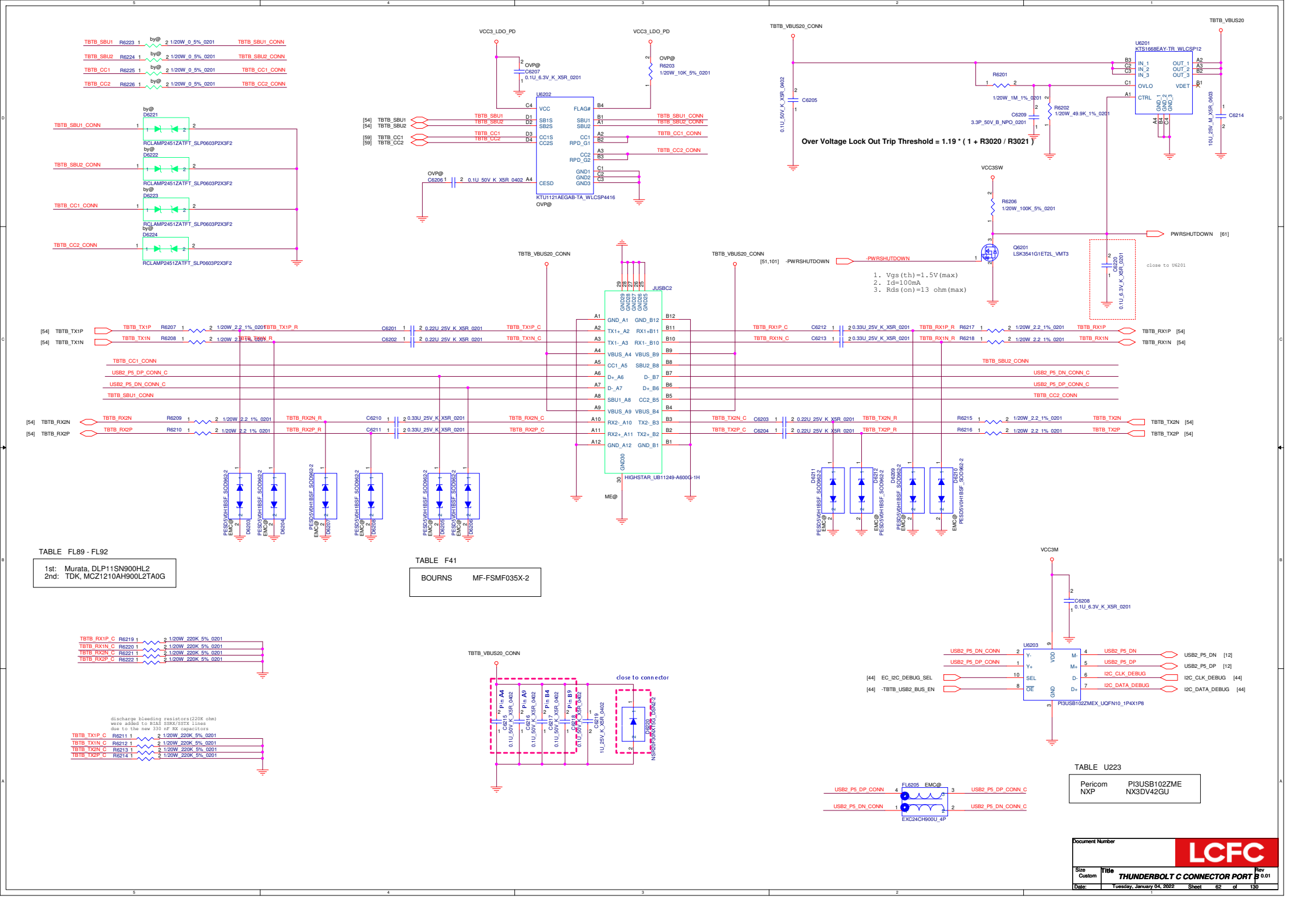
TBTB_SBU1 R6223 by@ 2 1/20W_0_5%_0201 TBTB_SBU1_CONN
TBTB_SBU2 R6224 by@ 2 1/20W_0_5%_0201 TBTB_SBU2_CONN
TBTB_CC1 R6225 by@ 2 1/20W_0_5%_0201 TBTB_CC1_CONN
TBTB_CC2 R6226 by@ 2 1/20W_0_5%_0201 TBTB_CC2_CONN
D6221 RCLAMP2451ZATFT_SLP0603P2X3F2
D6222 RCLAMP2451ZATFT_SLP0603P2X3F2
D6223 RCLAMP2451ZATFT_SLP0603P2X3F2
D6224 RCLAMP2451ZATFT_SLP0603P2X3F2
VCC3_LDO_PD
C6207 OVP@ 0.1U_6.3V_K_X5R_0201
R6203 OVP@ 1/20W_10K_5%_0201
U6202 KTU1121AEGAB-TA_WLCSP4416
C6205 OVP@ 0.1U_50V_K_X5R_0402
TBTB_VBUS20_CONN
C6205 0.1U_50V_K_X5R_0402
U6201 KTS1668EAY-TR_WLCSP12
R6201 1/20W_1M_1%_0201
R6202 1/20W_49.9K_1%_0201
C6209 3.3P_50V_B_NPO_0201
C6214 10U_25V_M_X5R_0603
Over Voltage Lock Out Trip Threshold = 1.19 * (1 + R3020 / R3021)
VCC3SW
R6206 1/20W_100K_5%_0201
Q6201 LSK3541G1ET2L_VMT3
PWRSHUTDOWN [61]
C6220 0.1U_6.3V_K_X5R_0201
close to U6201
-PWRSHUTDOWN
1. Vgs(th)=1.5V(max)
2. Id=100mA
3. Rds(on)=13 ohm(max)
JUSBC2
HIGHSTAR_UB11249-A600C-1H
TBTB_TX1P R6207 2 1/20W_2.2_1%_0201 TBTB_TX1P_R
TBTB_TX1N R6208 2 1/20W_2.2_1%_0201 TBTB_TX1N_R
C6201 2 0.22U_25V_K_X5R_0201 TBTB_TX1P_C
C6202 2 0.22U_25V_K_X5R_0201 TBTB_TX1N_C
TBTB_RX1P_C C6212 2 0.33U_25V_K_X5R_0201 TBTB_RX1P_R R6217 2 1/20W_2.2_1%_0201 TBTB_RX1P
TBTB_RX1N_C C6213 2 0.33U_25V_K_X5R_0201 TBTB_RX1N_R R6218 2 1/20W_2.2_1%_0201 TBTB_RX1N
TBTB_RX2N R6209 2 1/20W_2.2_1%_0201 TBTB_RX2N_R
TBTB_RX2P R6210 2 1/20W_2.2_1%_0201 TBTB_RX2P_R
C6210 2 0.33U_25V_K_X5R_0201 TBTB_RX2N_C
C6211 2 0.33U_25V_K_X5R_0201 TBTB_RX2P_C
TBTB_TX2N_C C6203 2 0.22U_25V_K_X5R_0201 TBTB_TX2N_R R6215 2 1/20W_2.2_1%_0201 TBTB_TX2N
TBTB_TX2P_C C6204 2 0.22U_25V_K_X5R_0201 TBTB_TX2P_R R6216 2 1/20W_2.2_1%_0201 TBTB_TX2P
PESD5V0H1BSF_SOD962-2
D6203 D6204 D6207 D6208 D6205 D6206 D6211 D6212 D6209 D6210
TBTB_CC1_CONN
USB2_P5_DP_CONN_C
USB2_P5_DN_CONN_C
TBTB_SBU1_CONN
TBTB_SBU2_CONN
TBTB_CC2_CONN
TABLE FL89 - FL92
1st: Murata, DLP11SN900HL2
2nd: TDK, MCZ1210AH900L2TA0G
TABLE F41
BOURNS MF-FSMF035X-2
TBTB_RX1P_C R6219 1/20W_220K_5%_0201
TBTB_RX1N_C R6220 1/20W_220K_5%_0201
TBTB_RX2N_C R6221 1/20W_220K_5%_0201
TBTB_RX2P_C R6222 1/20W_220K_5%_0201
discharge bleeding resistors(220K ohm)
were added to BIAS SSRX/SSTX lines
due to the new 330 nF RX capacitors
TBTB_TX1P_C R6211 1/20W_220K_5%_0201
TBTB_TX1N_C R6212 1/20W_220K_5%_0201
TBTB_TX2N_C R6213 1/20W_220K_5%_0201
TBTB_TX2P_C R6214 1/20W_220K_5%_0201
close to connector
C6215 Pin A4 0.1U_50V_K_X5R_0402
C6216 Pin A9 0.1U_50V_K_X5R_0402
C6217 Pin B4 0.1U_50V_K_X5R_0402
C6218 Pin B9 0.1U_50V_K_X5R_0402
C6219 1U_25V_K_0402
D6220 NSR20F30NXT5G_DSN2-2
VCC3M
C6208 0.1U_6.3V_K_X5R_0201
U6203 PI3USB102ZMEX_UQFN10_1P4X1P8
USB2_P5_DN_CONN
USB2_P5_DP_CONN
EC_I2C_DEBUG_SEL
-TBTB_USB2_BUS_EN
USB2_P5_DN [12]
USB2_P5_DP [12]
I2C_CLK_DEBUG [44]
I2C_DATA_DEBUG [44]
FL6205 EMC@ EXC24CH900U_4P
TABLE U223
Pericom PI3USB102ZME
NXP NX3DV42GU
Document Number
LCFC
Size Custom
Title THUNDERBOLT C CONNECTOR PORT B
Rev 0.01
Date: Tuesday, January 04, 2022
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Project Name : T14s Gen2	Title : BLANK
Size : C	Document Number :
	Rev : 0.1
Date: Tuesday, January 04, 2022	Sheet : 63 of 130

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Size : C	Document Number :
	Rev : 0.1
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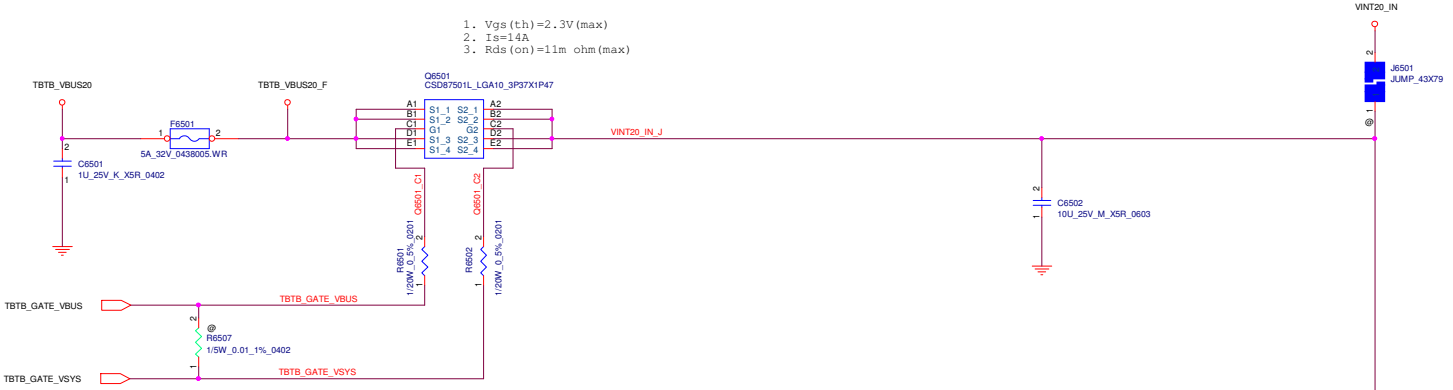

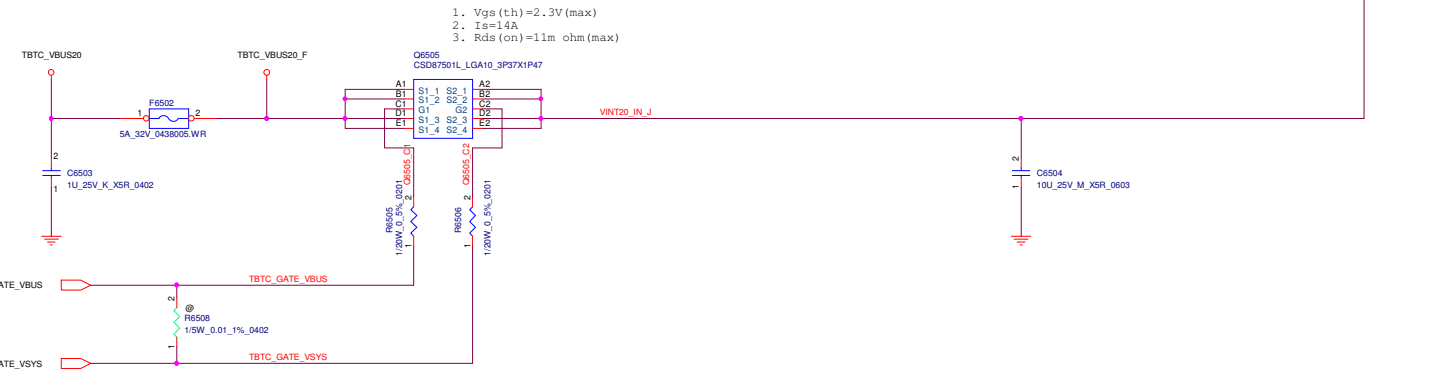

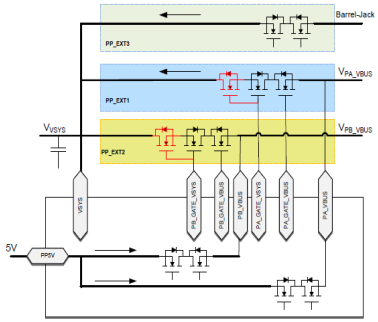

Document Number	LCFC	
Size: Custom	Title: 065_TYPEC_DCIN	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 65 of 130	

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Project Name : T14s Gen2	Title : BLANK
Size : C	Document Number :
Rev : 0.1	
Date: Tuesday, January 04, 2022	Sheet : 66 of 130

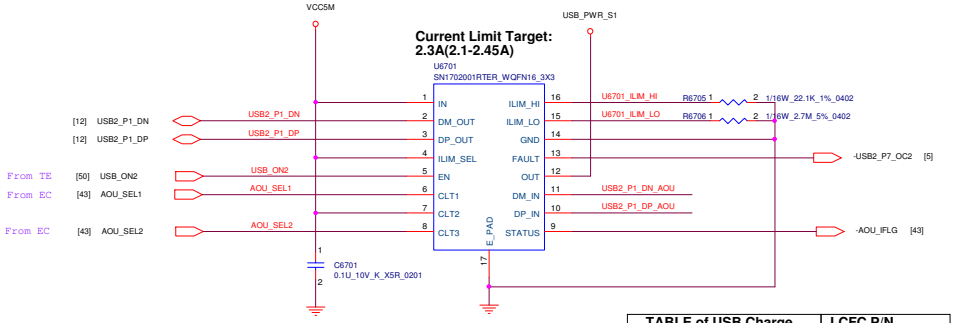
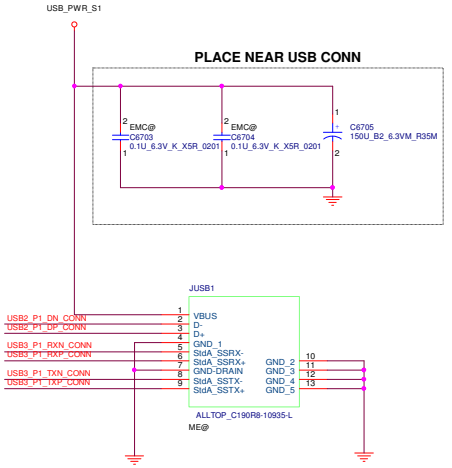
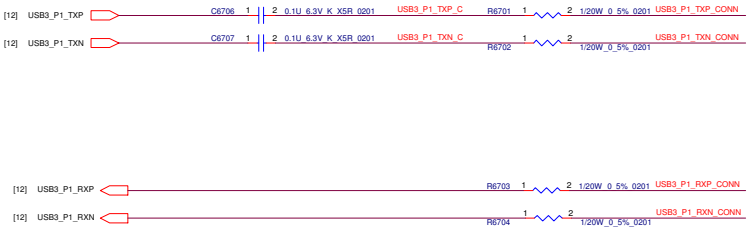
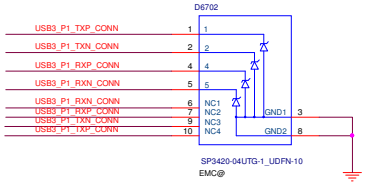
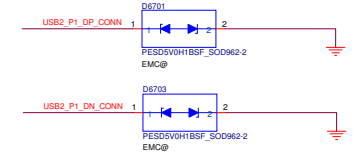


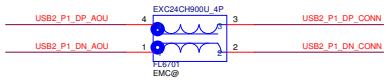
TABLE of USB Charge		LCFC P/N
TI	SN1702001RTER	SA00008HF00











Security Classification	LC Future Center Secret Data		
Issued Date	2019/01/12	Deciphered Date	2019/04/12

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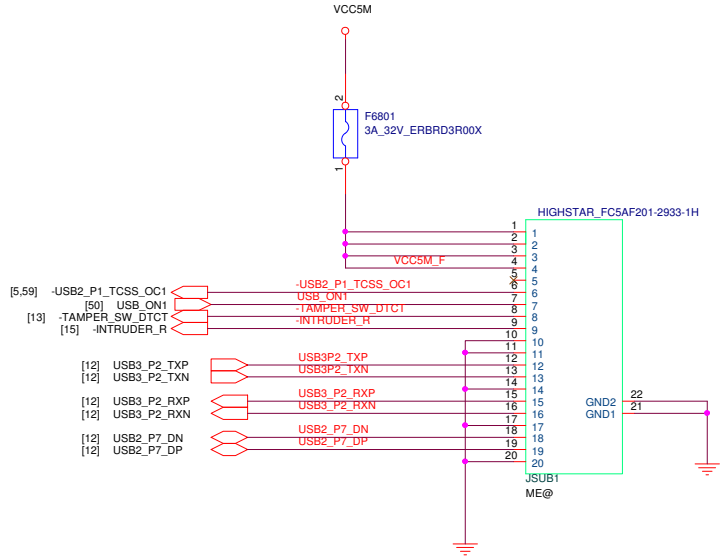
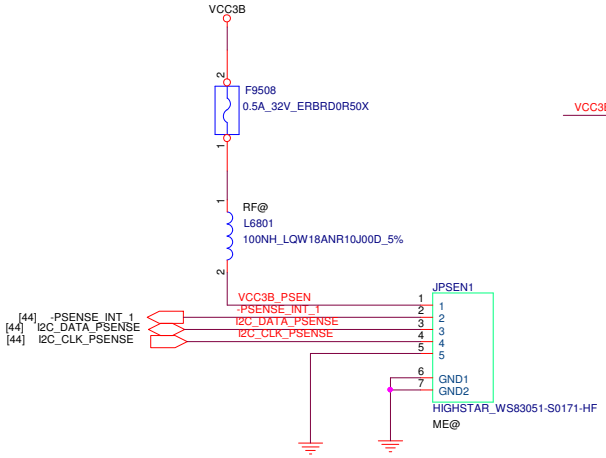
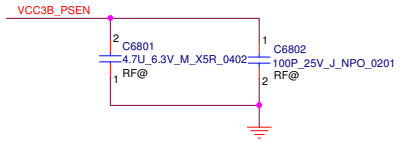
Title	USB TYPE-A CONNECTOR		
Size: Custom	Document Number: T14s Gen2		Rev: 0.1
Date: Tuesday, January 04, 2022	Sheet 67 of 130		







P-sensor IC

WLCSP-9

(Channel 0)

Ping number	MB Net name	P-IC Net name
1	VCC3B_PSEN_3.3V	VDDHI
2	-PSENSE_INT_1	GPIO/RDY
3	I2C_DATA_PSENSE	SDA
4	I2C_CLK_PSENSE	SCL
5	GND	VSS

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Issued Date	2019/01/12	Deciphered Date	2019/04/12

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Title: USB TYPE-A CONNECTOR

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Project Name : T14s Gen2	Title : BLANK
Size : C	Document Number :
Rev : 0.1	
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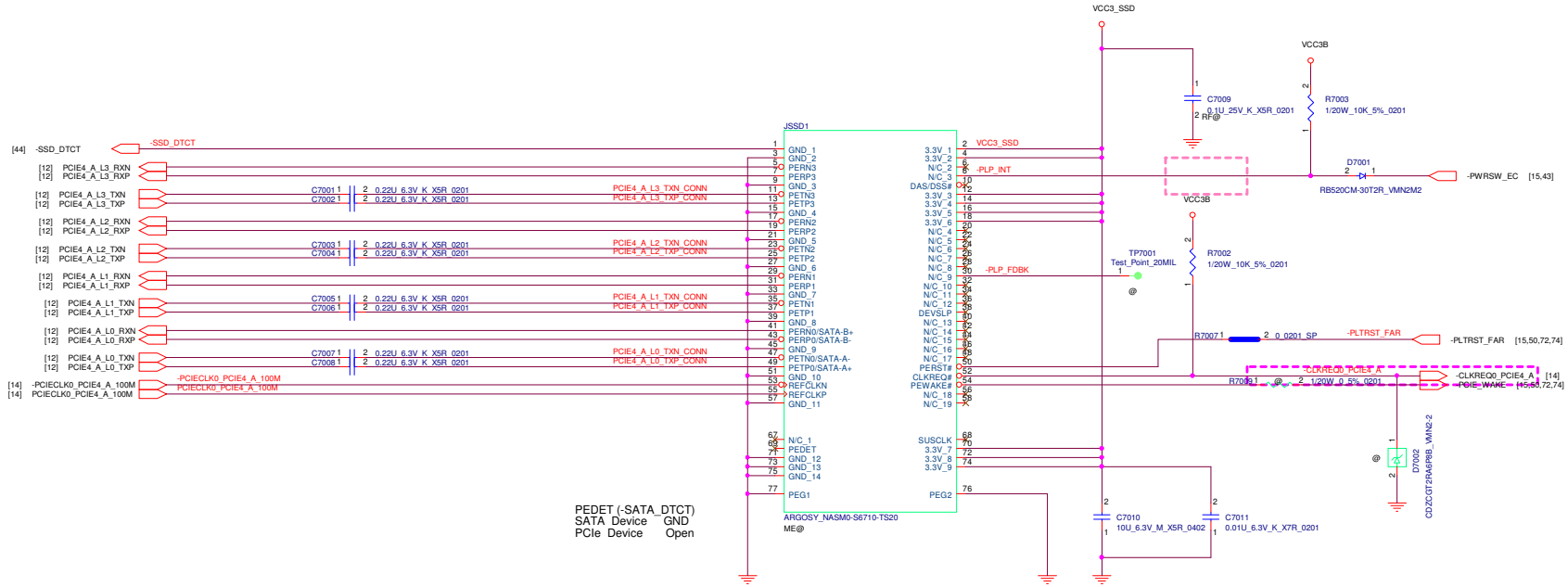
M.2 Socket 3 (Key-M) for 2280 S3 SSD

H=2.65mm Connector



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Rev: 0.01	
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Project Name : T14s Gen2	Title : BLANK
Size : C	Document Number :
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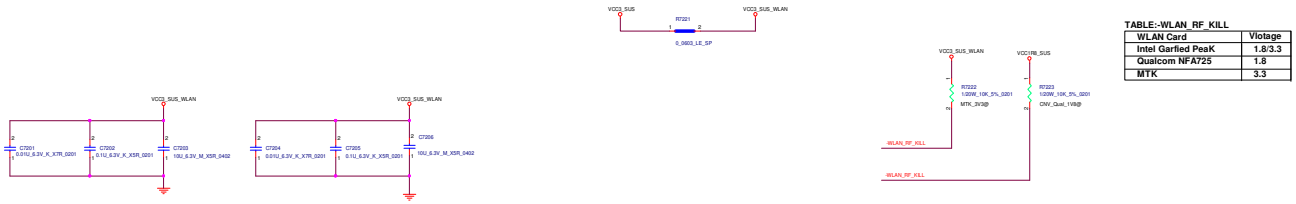

TABLE:-WLAN_RF_KILL

WLAN Card	Vlotage
Intel Garfied PeaK	1.8/3.3
Qualcom NFA725	1.8
MTK	3.3

M.2 Type 1216 Module for WLAN / Bluetooth

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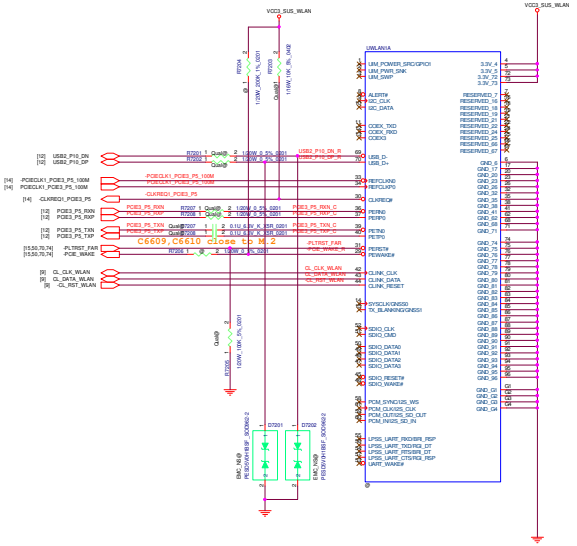
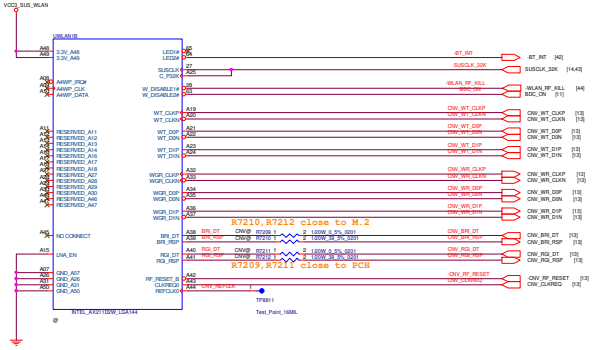
TABLE

Companion RF (CRF)	CNVio	REFCLK	CLKREQ
Jefferson Peak (JfP)	Gen1	Supported	Supported
Harrison Peak (HrP)	Gen2	Not Supported	Not Supported
Garfield Peak 2 (GfP2)	Gen2	Not Supported	Not Supported

TABLE

Platform	CNVio	PCH IP	REFCLK
Whiskey Lake	Gen1	Pulsar	38.4MHz Clock form JfP Module
Ice Lake	Gen2	Quasar	Generated inside SoC
Alder Lake	Gen2	Solar	Generated inside SoC

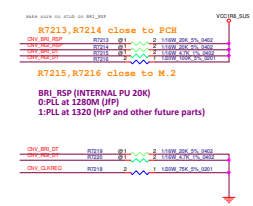




R6602 close to M.2

CNV_RGI_DT
0:CNVI ENABLE
1:CNVI DISABLE

CNV_BRI_DT
0:38.4/19.2MHz (DEFAULT) - INTERNAL PD20K
1:24MHZ



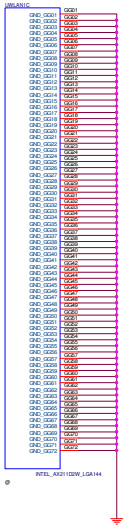
R7213,R7214 close to PCH

R7215,R7216 close to M.2

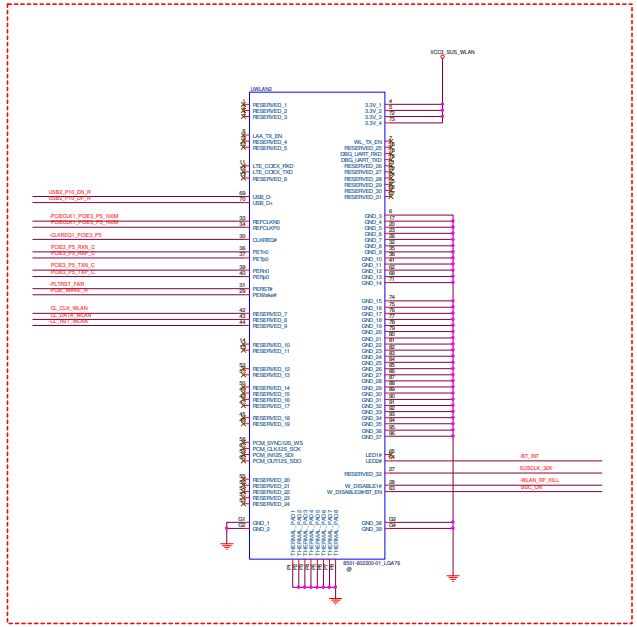
BRI_RSP (INTERNAL PU 20K)
0:PLL at 1280M (JfP)
1:PLL at 1320 (HrP and other future parts)

R7210,R7212 close to M.2

R7209,R7211 close to PCH



Co-lay with UWLAN1



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Project Name : T14s Gen2	Title : BLANK
Size : C	Document Number :
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M.2 Socket 2 (Key-B) for 3052 S3 WWAN

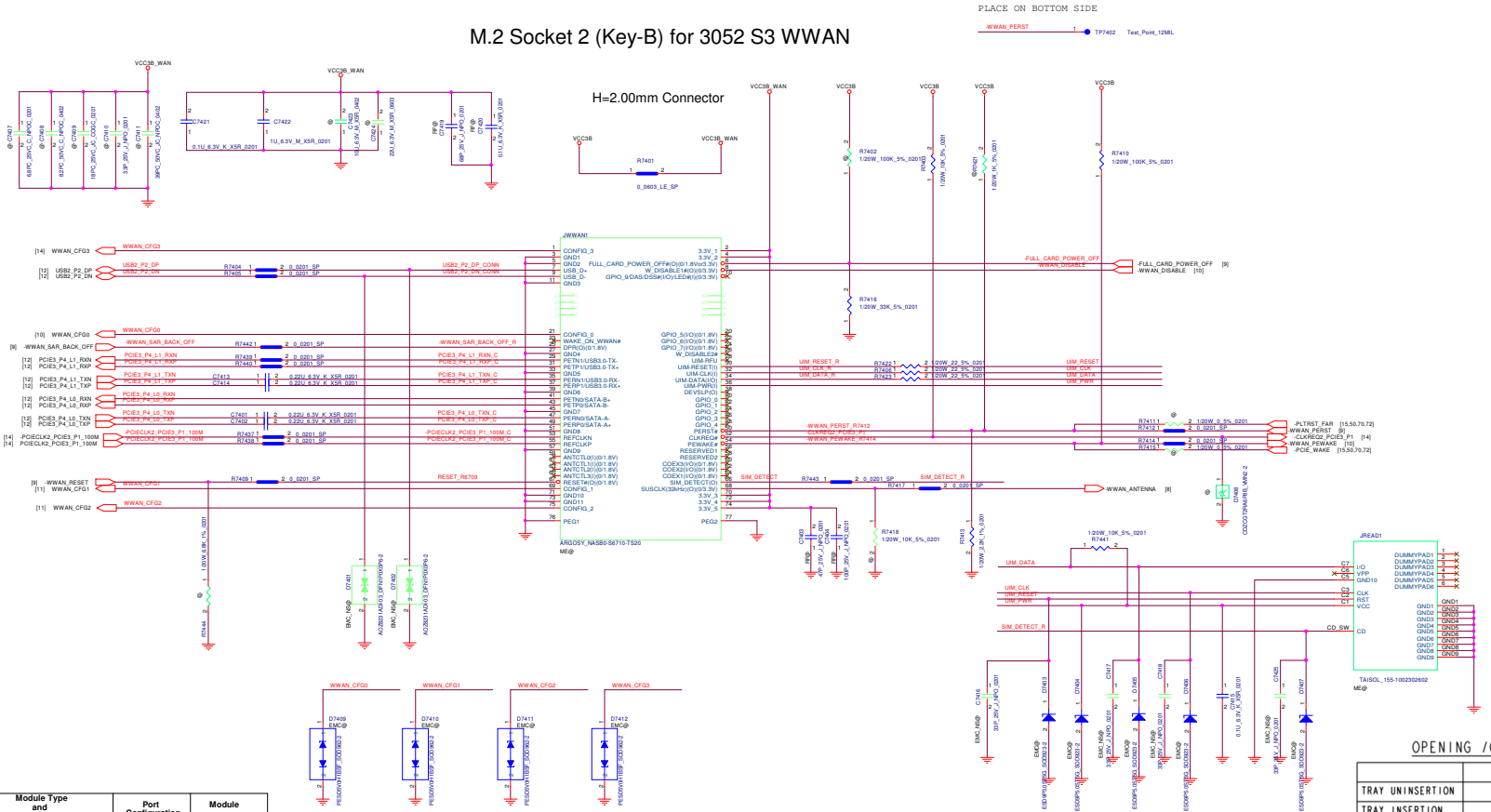


TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration	Module
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)			
0	GND	GND	GND	GND	SSD - SATA	N/A	
1	GND	GND	GND	NC	SSD - PCIe	N/A	
2	GND	GND	NC	GND	WWAN - PCIe	0	
3	GND	GND	NC	NC	WWAN - PCIe	1	
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0	
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1	
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2	
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3	FM350-GL
8	NC	GND	GND	GND	WWAN - SSIC	0	EM05-CE EM05-G
9	NC	GND	GND	NC	WWAN - SSIC	1	
10	NC	GND	NC	GND	WWAN - SSIC	2	
11	NC	GND	NC	NC	WWAN - SSIC	3	
12	NC	NC	GND	GND	WWAN - PCIe	2	
13	NC	NC	GND	NC	WWAN - PCIe	3	
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined	L860-GL
15	NC	NC	NC	NC	No Module Present	N/A	

TABLE of WWAN (Pin68# ANT_CONFIG)		
M.2 module side	Description	MIMO mode
EM05-G	TBD	TBD
L860 R+	#68=NC/high	2
	#68=low level	4

EM05-G EM05-CE

	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3
EM05-CE	NC	GND	GND	GND
EM05-G	NC	GND	GND	GND

FM350-GL

Fibocom

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	NC	NC	NC	WWAN-PCIe Gen3, USB3.1 Gen1	Vendor defined

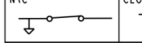
L860-GL

The M.2 module configuration is shown in the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	WWAN - PCIe Gen2	Vendor defined

OPENING /CLOSE OF SWITCH

	SWITCH FOR TRAY DETECT
TRAY UNINSERTION	CLOSE
TRAY INSERTION	OPEN



SIM Not Detect	SIM_DETECT	Project	Invert	Without Tray	Tray Mated
Low	High	JG2	Need	Open(High)	Close(Low)
Low	High	Phoenix	No need	Close(Low)	Open(High)

LCFC

Document Number		Rev
Size D	Title 074_M.2 SOCKET 2 MODULE M	0.01
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Size	Document Number		Rev
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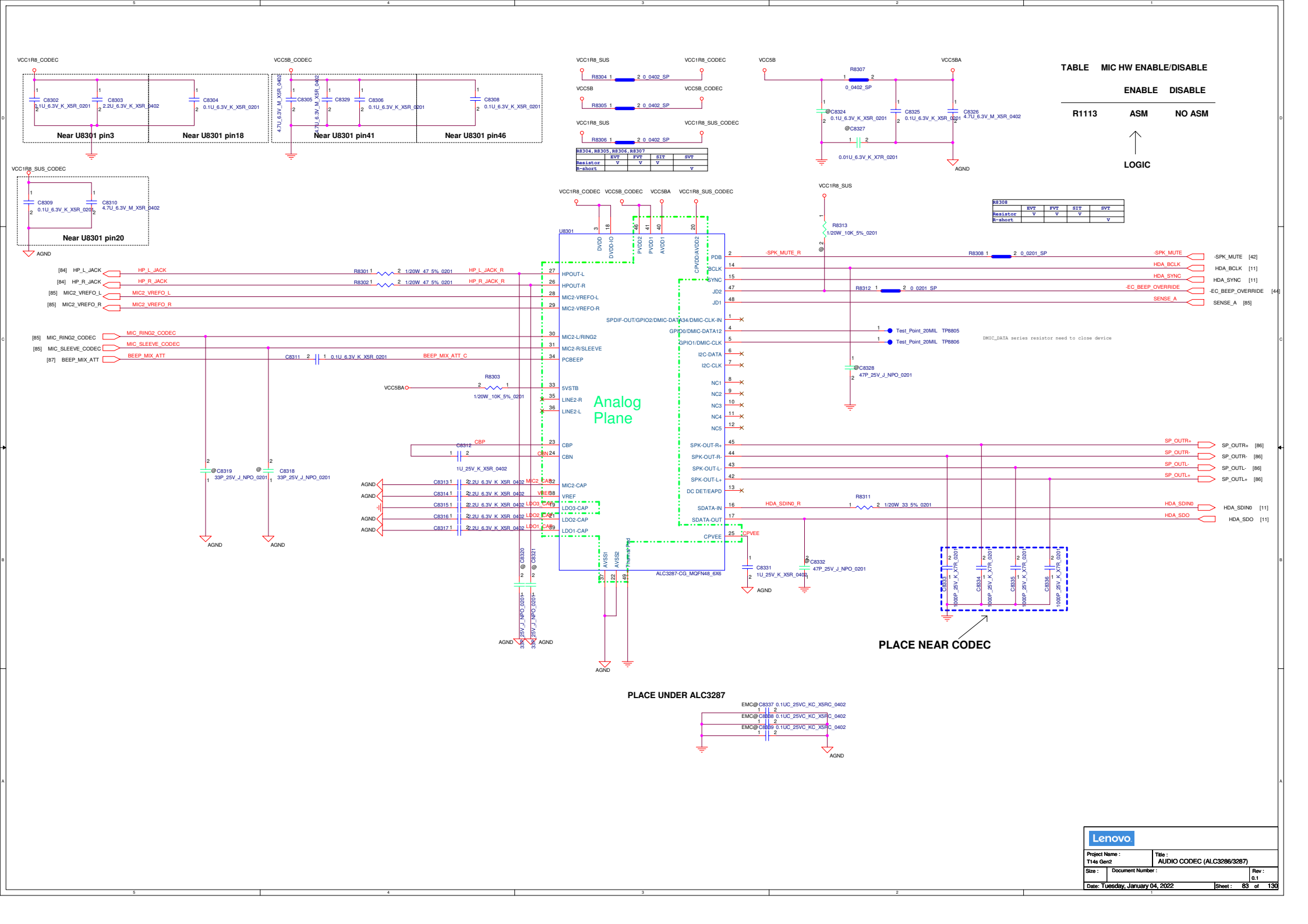
VCC1R8_CODEC
C8302 1U_6.3V_K_X5R_0201
C8303 2.2U_6.3V_K_X5R_0402
C8304 0.1U_6.3V_K_X5R_0201
Near U8301 pin3
Near U8301 pin18
VCC5B_CODEC
C8305 4.7U_6.3V_M_X5R_0402
C8329 2.7U_6.3V_K_X5R_0402
C8306 0.1U_6.3V_K_X5R_0201
C8308 0.1U_6.3V_K_X5R_0201
Near U8301 pin41
Near U8301 pin46
VCC1R8_SUS_CODEC
C8309 0.1U_6.3V_K_X5R_0201
C8310 4.7U_6.3V_M_X5R_0402
Near U8301 pin20
AGND
VCC1R8_SUS
R8304 0_0402_SP
VCC1R8_CODEC
VCC5B
R8305 0_0402_SP
VCC5B_CODEC
VCC1R8_SUS
R8306 0_0402_SP
VCC1R8_SUS_CODEC
R8304,R8305,R8306,R8307
EVT | EVT | SIT | SVT
Resistor | V | V | V |
R-short | | | | V
VCC5B
R8307 0_0402_SP
VCC5BA
@C8324 0.1U_6.3V_K_X5R_0201
C8325 0.1U_6.3V_K_X5R_0201
C8326 4.7U_6.3V_M_X5R_0402
@C8327 0.01U_6.3V_K_X7R_0201
AGND
TABLE MIC HW ENABLE/DISABLE
ENABLE DISABLE
R1113 ASM NO ASM
LOGIC
VCC1R8_CODEC VCC5B_CODEC VCC5BA VCC1R8_SUS_CODEC
U8301
DVDD DVDD-IO PVDD2 PVDD1 AVDD1 CPVDD/AVDD2
VCC1R8_SUS
R8313 1/20W_10K_5%_0201
R8308
EVT | EVT | SIT | SVT
Resistor | V | V | V |
R-short | | | | V
[84] HP_L_JACK HP_L_JACK
[84] HP_R_JACK HP_R_JACK
[85] MIC2_VREFO_L MIC2_VREFO_L
[85] MIC2_VREFO_R MIC2_VREFO_R
R8301 1/20W_47_5%_0201 HP_L_JACK_R
R8302 1/20W_47_5%_0201 HP_R_JACK_R
HPOUT-L
HPOUT-R
MIC2-VREFO-L
MIC2-VREFO-R
SPDIF-OUT/GPIO2/DMIC-DATA34/DMIC-CLK-IN
GPIO0/DMIC-DATA12
GPIO1/DMIC-CLK
I2C-DATA
I2C-CLK
NC1
NC2
NC3
NC4
NC5
PDB
BCLK
SYNC
JD2
JD1
-SPK_MUTE_R
R8308 0_0201_SP
-SPK_MUTE
HDA_BCLK
HDA_SYNC
-EC_BEEP_OVERRIDE
SENSE_A
-SPK_MUTE [42]
HDA_BCLK [11]
HDA_SYNC [11]
-EC_BEEP_OVERRIDE [44]
SENSE_A [85]
R8312 0_0201_SP
Test_Point_20MIL TP8805
Test_Point_20MIL TP8806
DMIC_DATA series resistor need to close device
@C8328 47P_25V_J_NPO_0201
[85] MIC_RING2_CODEC MIC_RING2_CODEC
[85] MIC_SLEEVE_CODEC MIC_SLEEVE_CODEC
[87] BEEP_MIX_ATT BEEP_MIX_ATT
C8311 0.1U_6.3V_K_X5R_0201 BEEP_MIX_ATT_C
MIC2-L/RING2
MIC2-R/SLEEVE
PCBEEP
R8303 1/20W_10K_5%_0201
VCC5BA
5VSTB
LINE2-R
LINE2-L
Analog Plane
C8312 CBP CBN 1U_25V_K_X5R_0402
CBP
CBN
@C8319 33P_25V_J_NPO_0201
@C8318 33P_25V_J_NPO_0201
AGND
C8313 2.2U_6.3V_K_X5R_0402 MIC2_CAP
C8314 2.2U_6.3V_K_X5R_0402 VREF
C8315 2.2U_6.3V_K_X5R_0402 LDO3_CAP
C8316 2.2U_6.3V_K_X5R_0402 LDO2_CAP
C8317 2.2U_6.3V_K_X5R_0402 LDO1_CAP
MIC2-CAP
VREF
LDO3-CAP
LDO2-CAP
LDO1-CAP
@C8320 33P_25V_J_NPO_0201
@C8321 33P_25V_J_NPO_0201
AVSS1
AVSS2
Thermal Pad
ALC3287-CG_MQFN48_6X6
SPK-OUT-R+
SPK-OUT-R-
SPK-OUT-L-
SPK-OUT-L+
DC DET/EAPD
SDATA-IN
SDATA-OUT
CPVEE
HDA_SDIN0_R
R8311 1/20W_33_5%_0201
SP_OUTR+
SP_OUTR-
SP_OUTL-
SP_OUTL+
HDA_SDIN0
HDA_SDO
SP_OUTR+ [86]
SP_OUTR- [86]
SP_OUTL- [86]
SP_OUTL+ [86]
HDA_SDIN0 [11]
HDA_SDO [11]
CPVEE
C8331 1U_25V_K_X5R_0402
C8332 47P_25V_J_NPO_0201
C8333 1000P_25V_K_X7R_0201
C8334 1000P_25V_K_X7R_0201
C8335 1000P_25V_K_X7R_0201
C8336 1000P_25V_K_X7R_0201
PLACE NEAR CODEC
PLACE UNDER ALC3287
EMC@C8337 0.1UC_25VC_KC_X5RC_0402
EMC@C8338 0.1UC_25VC_KC_X5RC_0402
EMC@C8339 0.1UC_25VC_KC_X5RC_0402
AGND
Lenovo
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Title : AUDIO CODEC (ALC3286/3287)
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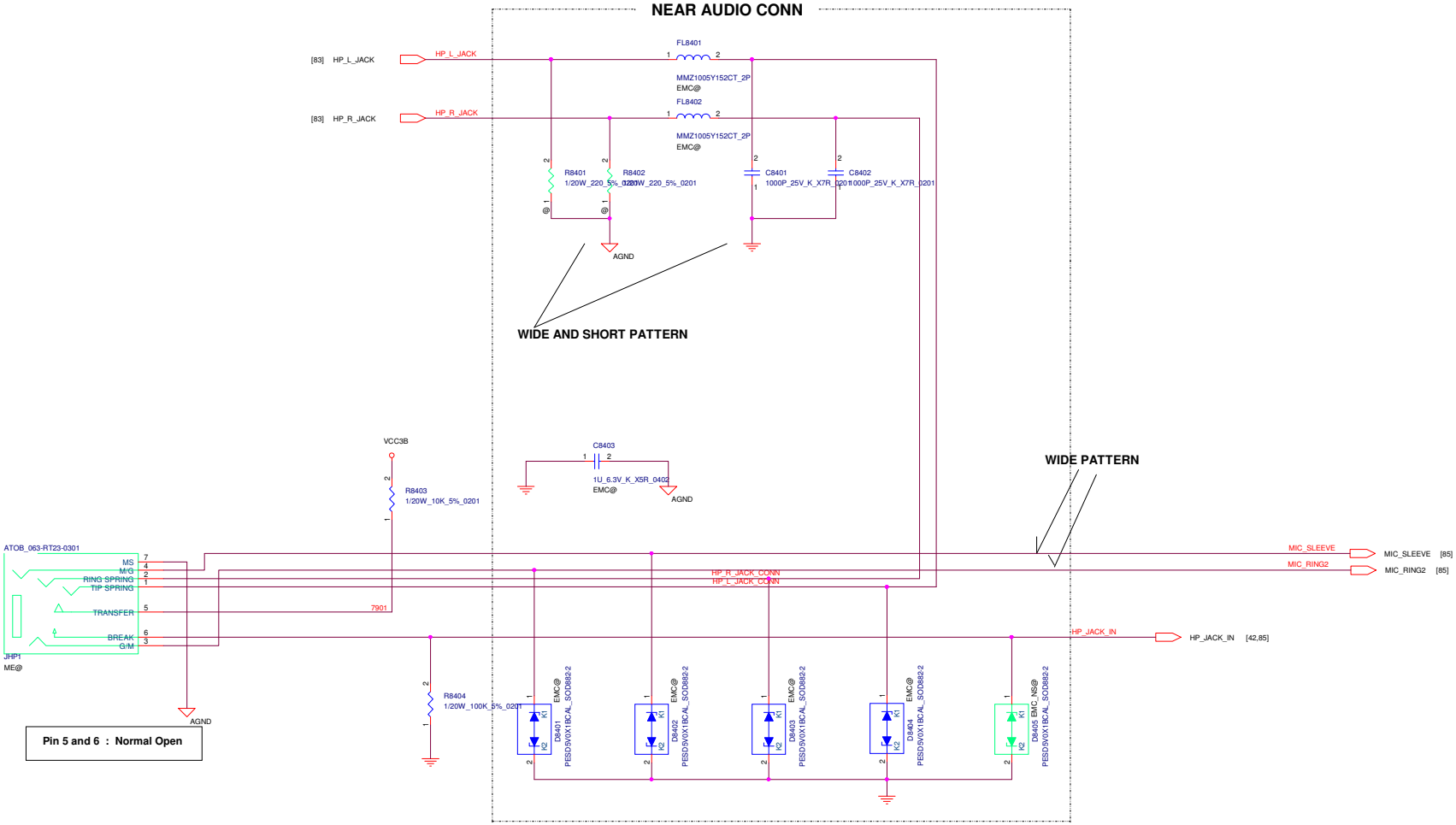

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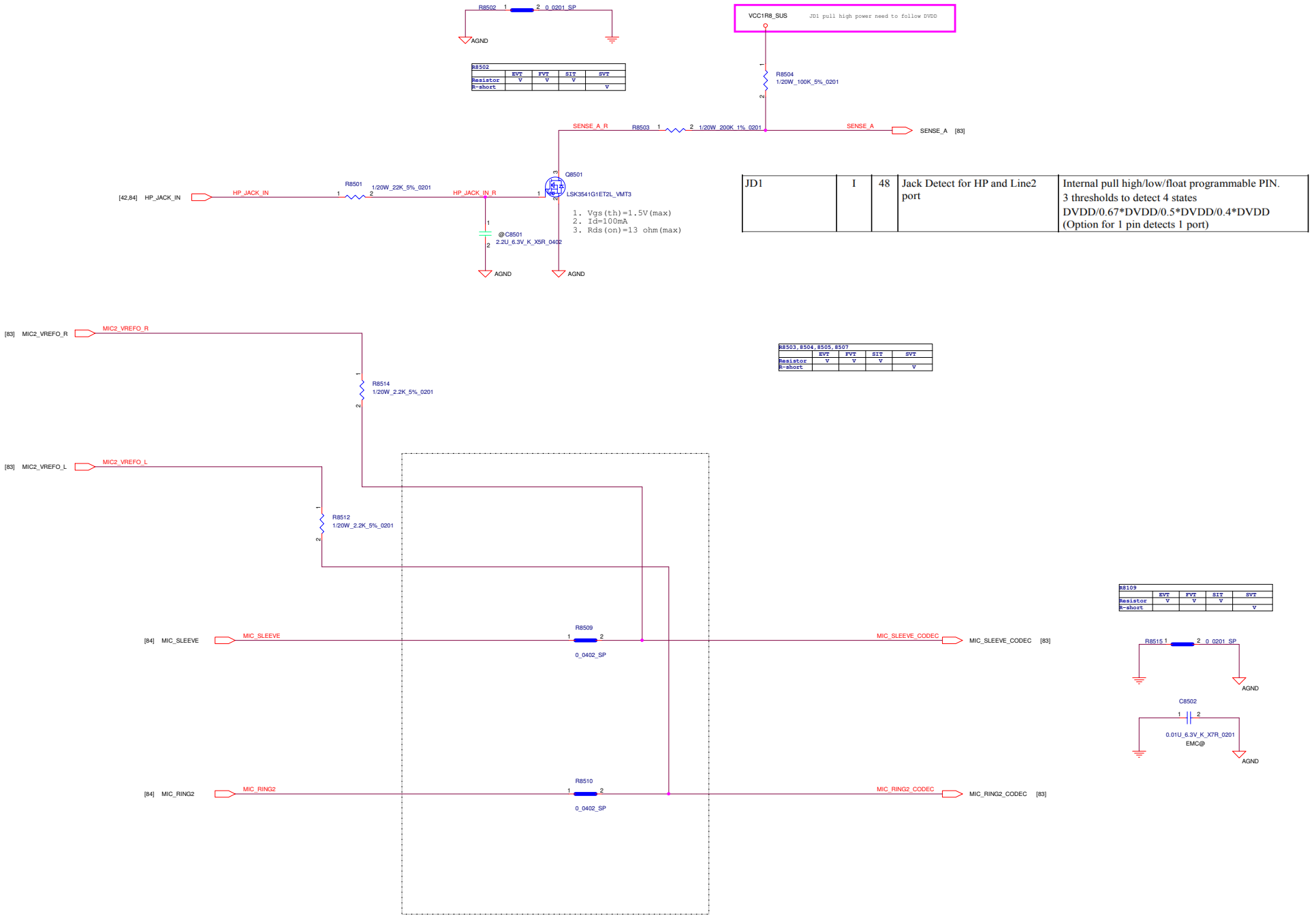

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Project Name : T14s Gen2	Title : AUDIO JACK SENSE_MIC_I/F
Size : C	Document Number :
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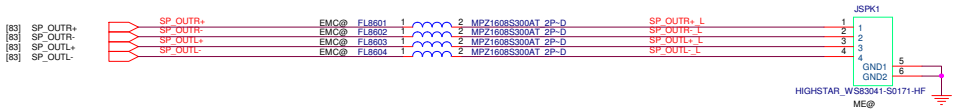

Project Name : T14s Gen2	Title : AUDIO SPEAKER	
Size : C	Document Number :	Rev : 0.1
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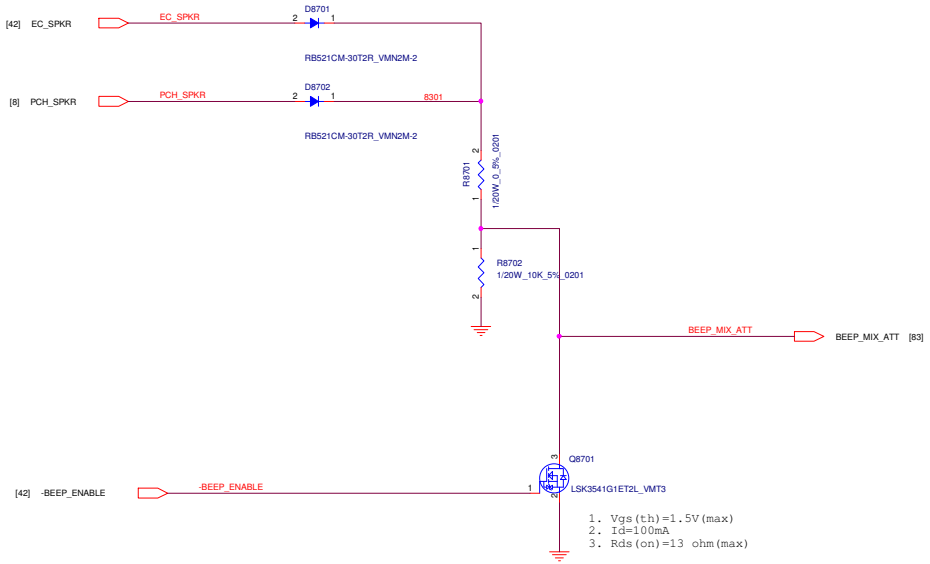

Project Name : T14s Gen2	Title : AUDIO BEEP
Size : C	Document Number :
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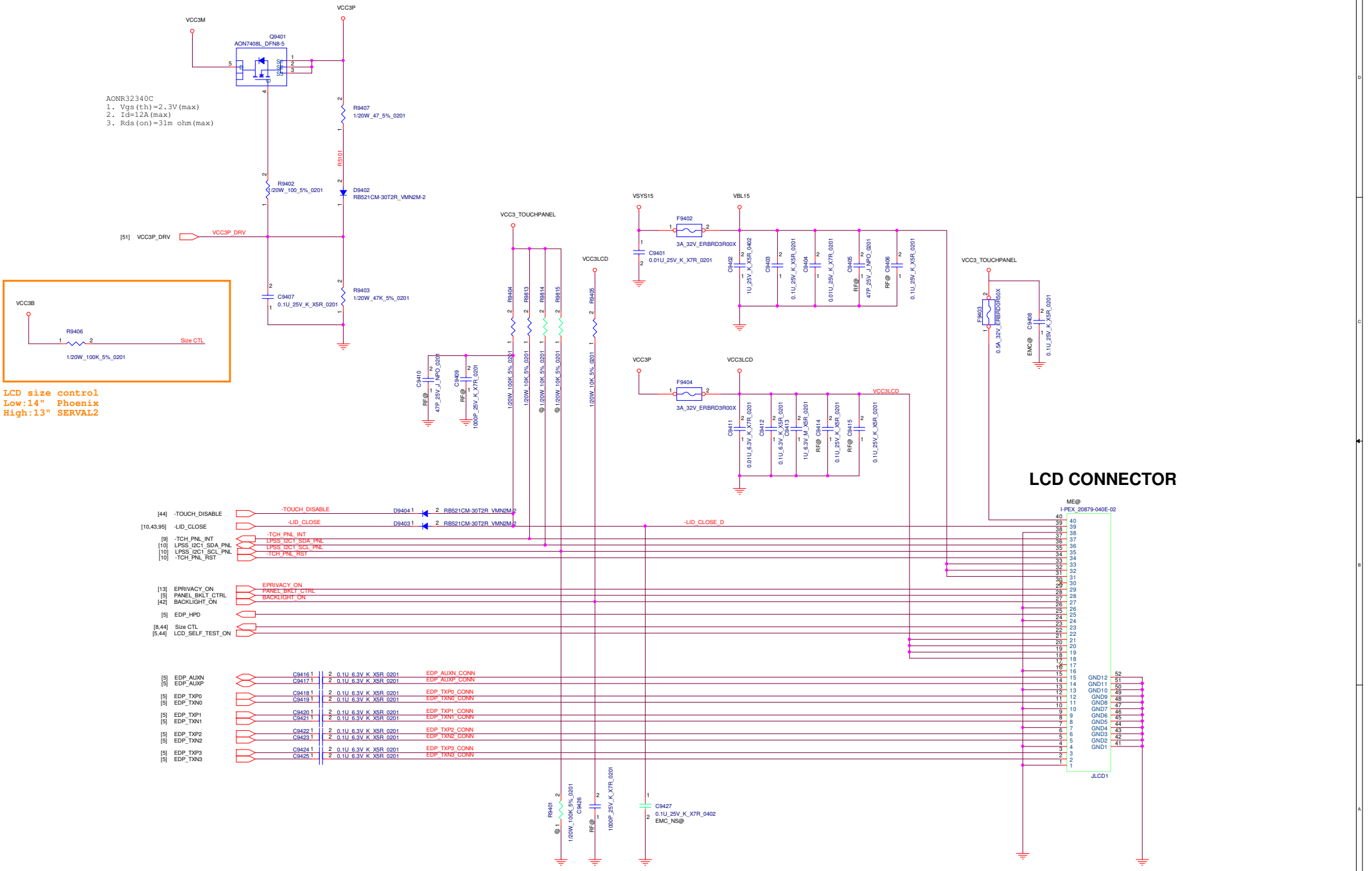

Security Classification	LC Future Center Secret Data		
Issued Date	2018/01/12	Deciphered Date	2018/01/12

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Title: LCD INTERFACE

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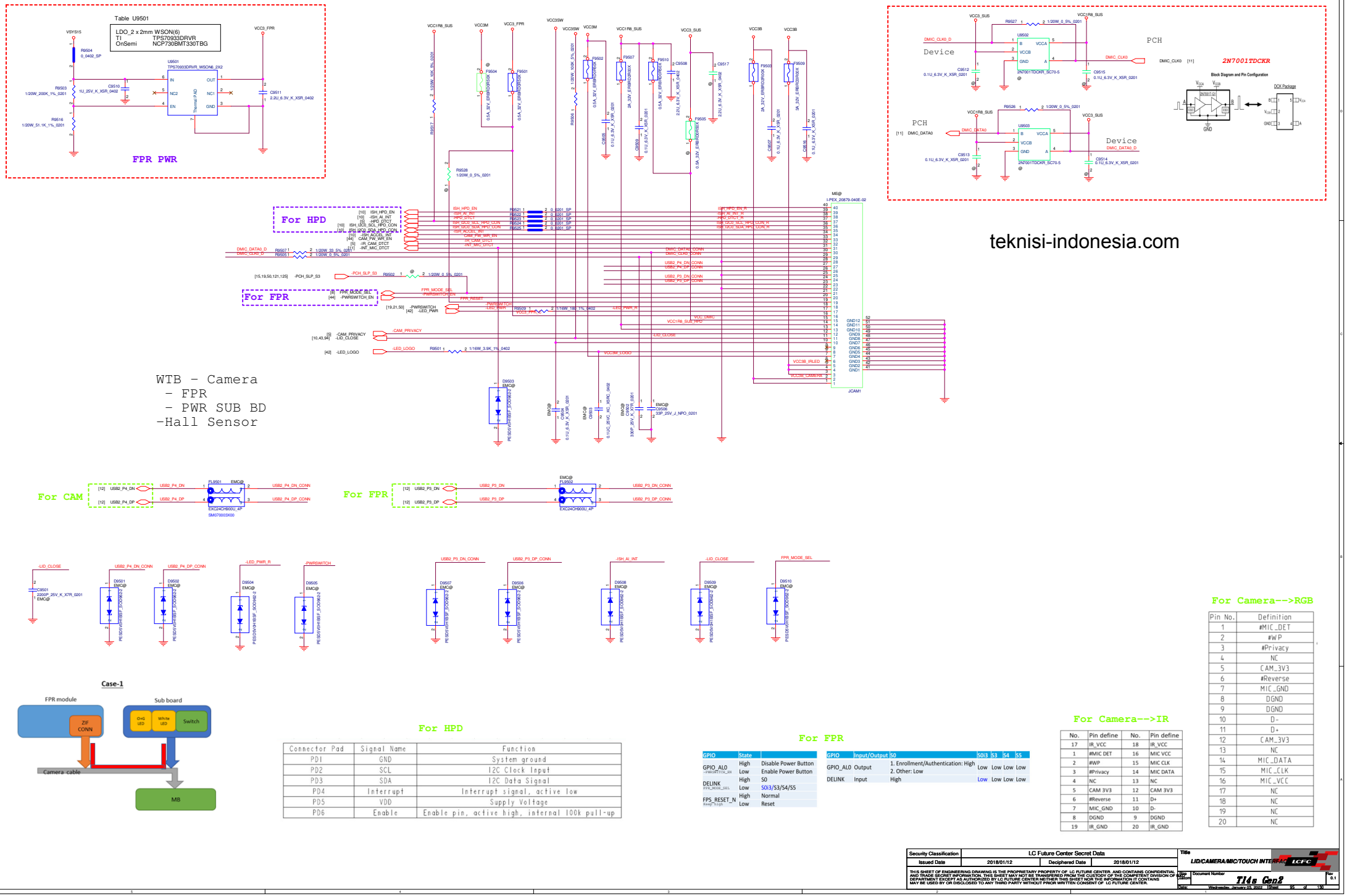

For HPD

Connector Pad	Signal Name	Function
PD1	GND	System ground
PD2	SCL	I2C Clock Input
PD3	SDA	I2C Data Signal
PD4	Interrupt	Interrupt signal, active low
PD5	VDD	Supply Voltage
PD6	Enable	Enable pin, active high, internal 100k pull-up

For FPR

GPIO	State	
GPIO_AL0	High	Disable Power Button
	Low	Enable Power Button
DELINK	High	S0
	Low	S0i3/S3/S4/S5
FPS_RESET_N	High	Normal
	Low	Reset

GPIO	Input/Output	S0	S0i3	S3	S4	S5
GPIO_AL0	Output	1: Enrollment/Authentication: High 2: Other: Low	Low	Low	Low	Low
DELINK	Input	High	Low	Low	Low	Low

For Camera-->IR

No.	Pin define	No.	Pin define
17	IR_VCC	18	IR_VCC
1	#MIC DET	16	MIC VCC
2	#WP	15	MIC CLK
3	#Privacy	14	MIC DATA
4	NC	13	NC
5	CAM 3V3	12	CAM 3V3
6	#Reverse	11	D+
7	MIC_GND	10	D-
8	DGND	9	DGND
19	IR_GND	20	IR_GND

For Camera-->RGB

Pin No.	Definition
1	#MIC_DET
2	#WP
3	#Privacy
4	NC
5	CAM_3V3
6	#Reverse
7	MIC_GND
8	DGND
9	DGND
10	D-
11	D+
12	CAM_3V3
13	NC
14	MIC_DATA
15	MIC_CLK
16	MIC_VCC
17	NC
18	NC
19	NC
20	NC

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Title: LID/CAMERA/MIC/TOUCH INTERFACE

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Title	<Title>	
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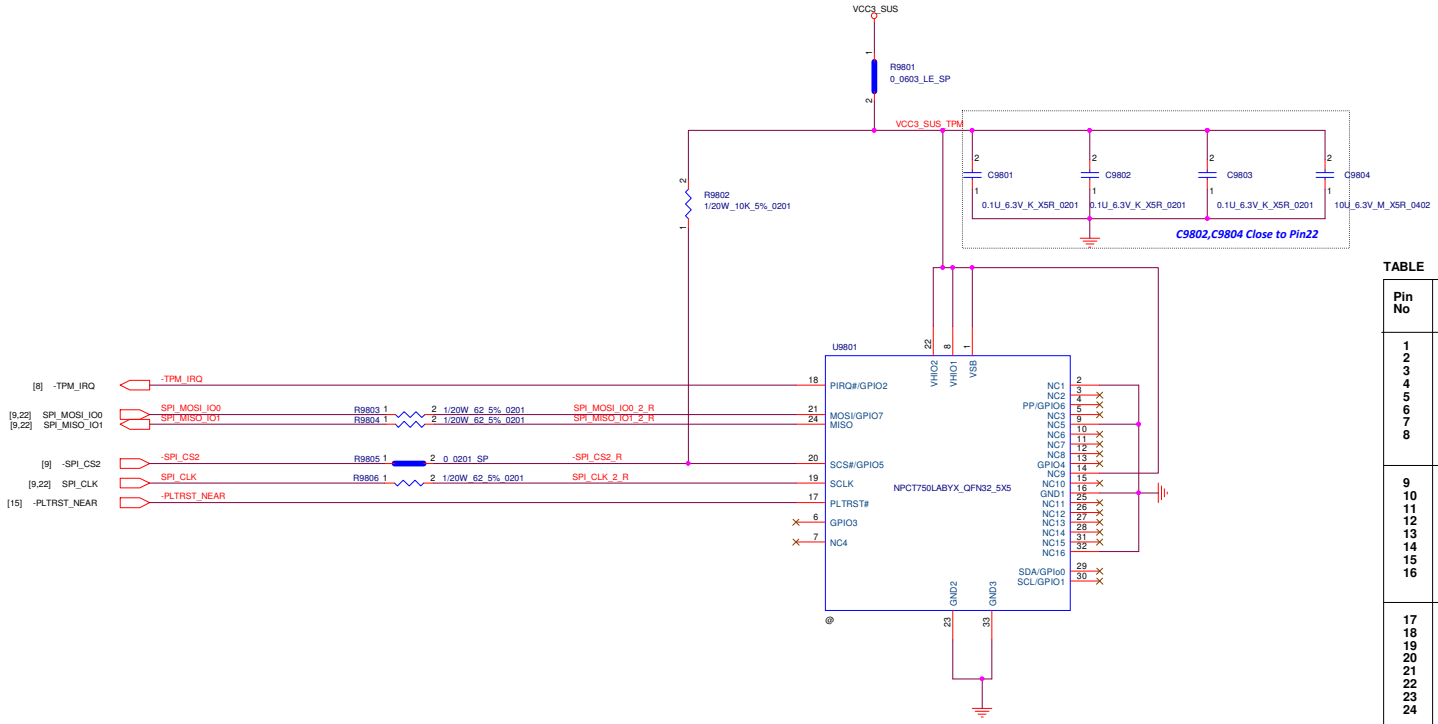

TABLE

Pin No	NATIONZ(X13) Z32H330TC-SQN-L4	Nuvoton NPCT760LAAYX	ST Micro ST33HTPH2X32AHE0	infineon SLB 9672VU2.0 FW15.21
1	VDD	VSB	NC	NCI/VDD
2	GND	NC	GND	GND
3	NC	NC	NC	NCI
4	NC	PP/GPIO6	PP	NCI
5	NC	NC	NC	NCI
6	NC	GPIO3	NC	GPIO
7	PP	NC	GPIO	PP
8	VDD	VHIO	NC	VDD
9	GND	NC	NC	GND
10	NC	NC	NC	NCI
11	NC	NC	NC	NCI
12	NC	NC	NC	NCI
13	GPIO	GPIO4	NC	NCI
14	VDD	NC	NC	NCI/VDD
15	NC	NC	NC	NCI
16	GND	GND	NC	NCI/VDD
17	SPI_RST#	PLTRST#	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#	CS#
21	MOSI	MOSI/GPIO7	MOSI	MOSI
22	VDD	VHIO	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NCI
26	NC	NC	NC	NCI
27	NC	NC	NC	NCI
28	NC	NC	NC	NCI
29	NC	SDA/GPIO0	NC	NC
30	NC	SCL/GPIO1	NC	NC
31	NC	NC	NC	NCI
32	GND	NC	NC	GND

TABLE of TPM (U9801)

	Vendor	P/N	LCFC P/N
After SIT USE	ST Micro	ST33HTPH2X32AHE0	SA0000C8600
	Nuvoton	NPCT760LAAYX	SA0000C3000
	NATIONZ (X13)	Z32H330TC-SQN-L4	SA0000C1S00
ONLY USE EVT	ST Micro	ST33HTPH2X32AHD8	SA0000AB720
	Nuvoton	NPCT750LADYX QFN	SA00008KS30
	infineon	SLB 9672VU2.0 FW15.21	SA0000C3310

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Title: DISCRETE TPM 2.0

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@H9
HOLEA
PAD_O8P5X8P0D3P9X3P4
CS22 Modify

@H11
HOLEA
PAD_C8P0D2P8
CS22 Modify

@H1
HOLEA
PAD_CT8P0D3P8
CS22 Modify

@H7
HOLEA
PAD_C6P0D3P0
CS22 Modify

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

@H24
HOLEA
PAD_C6P8

@H25
HOLEA
PAD_C6P8

@H26
HOLEA
PAD_C6P8

@H27
HOLEA
PAD_C6P8

CS22 Modify

@HICT1
HOLEA
PAD_C2P5D2P5N

@HICT2
HOLEA
PAD_C2P5D2P5N

@HICT3
HOLEA
PAD_C2P5D2P5N

@H28
HOLEA
PAD_C8P0D2P3
CS22 Modify

@H4
HOLEA
PAD_C8P0D2P3
CS22 Modify

@H29
HOLEA
PAD_O7P4X6D4P4X3

@H31
HOLEA
PAD_O6P5X5p3D3p5x2p3

@H18
HOLEA
PAD_C8P0D3P3
CS22 Modify

@H20
HOLEA
PAD_C8P0D3P3
CS22 Modify

@H22
HOLEA
PAD_C8P0D3P8
CS22 Modify

@H5
HOLEA
PAD_C5P0D2P3
CS22 Modify

@H34
HOLEA
PAD_C6P0D3P4
CS22 Modify

@H36
HOLEA
PAD_C2P3D2P3N

@H30
HOLEA
PAD_C3P0D3P0N

@H32
HOLEA
PAD_O0P8X2P5D0P8X2P5N

Title	<Title>	
Size A	Document Number T14s Gen2	Rev 0.1
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Document Number		LCFC
Size: Custom	Title: BLANK	Rev: 0.01
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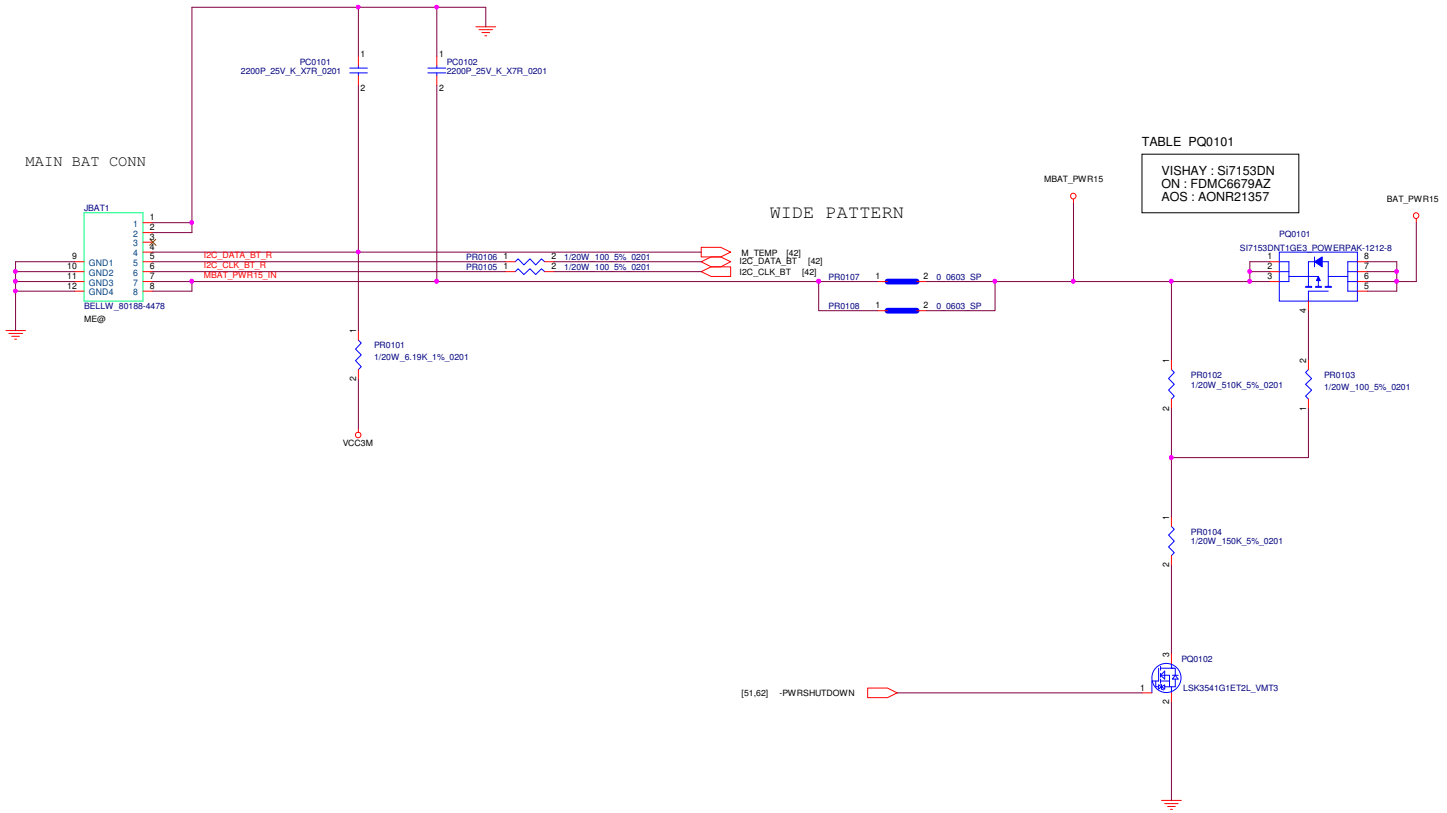

Document Number		LCFC
Size: Custom	Title: 101_BATTERY INPUT	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 101 of 130	

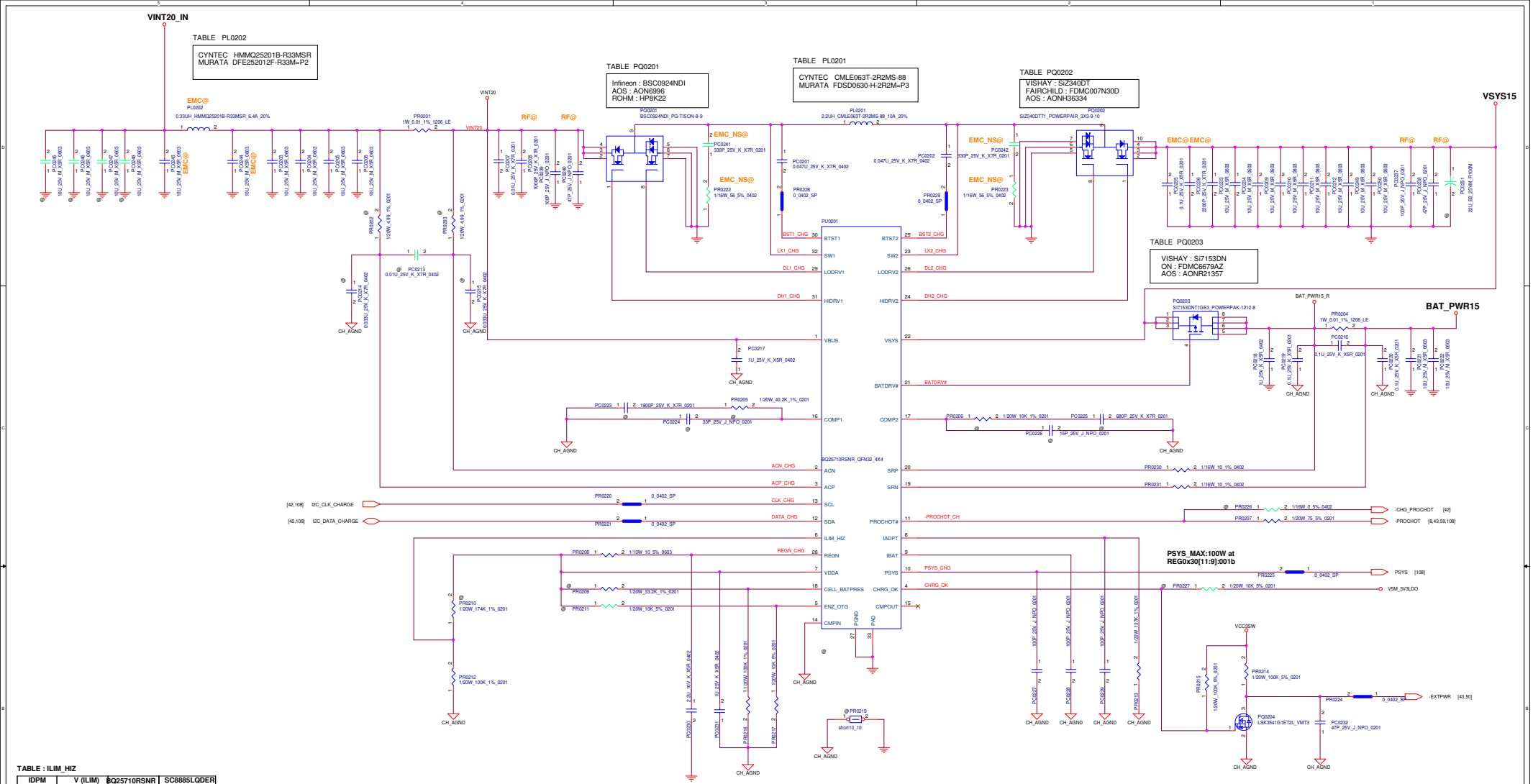

TABLE : ILIM_HIZ

IDPM	V (ILIM)	BQ25710RSNR	SC8885LQDER	
500mA	1.2V			
1.0A	1.4V			
1.5A	1.6V			
2.0A	1.8V	237K	191K	
3.0A	2.2V	174K	137K	← W/ 65W adapter
3.25A	2.3V	162K	127K	
4A	2.6V	131K		
5A	3V	100K		← W/ 100W adapter

TABLE : CELL_BATPRES (PR0209)

# of CELL	V (CELL_PRES)	BQ25710RSNR	SC8885LQDER	
1-CELL	1.5V	301K	249K	
2-CELL	2.5V	140K	110K	
3-CELL	3.5V	71.5K	49.9K	
4-CELL	4.5V	33.2K	16.5K	← LOGIC

TABLE

Inductor	R(IADP)	fsw@POR	
1.0uH	93kohm	800kHz	
2.2uH	137kohm	800kHz	← LOGIC
3.3uH	169kohm	800kHz	

Charger BOM table

IC	PU0201	BQ25710RSNR	SC8885LQDER
ACP	PR0202	4.99ohm_1%_0201	10ohm_1%_0201
ACN	PR0203	4.99ohm_1%_0201	10ohm_1%_0201
ACP	PC0214	0.033uF_10%_25V_0402	NO_ASM
ACN	PC0215	0.033uF_10%_25V_0402	NO_ASM
COMP1	PR0205	40.2k_1%_0201	100k_1%_0201
COMP1	PC0223	1800pF_10%_25V_0201	1000pF_10%_25V_0201
COMP1	PC0224	33pF_5%_25V_0201	10pF_5%_25V_0201
COMP2	PR0206	10k_1%_0201	330k_1%_0201
COMP2	PC0225	680pF_10%_25V_0201	1000pF_10%_25V_0201
COMP2	PC0226	15pF_5%_25V_0201	220pF_10%_25V_0201
ILIM_HIZ	PR0210	174k_1%_0201	137k_1%_0201
CELL_BATPRESZ	PR0209	33.2k_1%_0201	16.5k_1%_0201

← LOGIC

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Size: Custom	Title: BATTERY CHARGER(BQ25710)		Rev: 0.01
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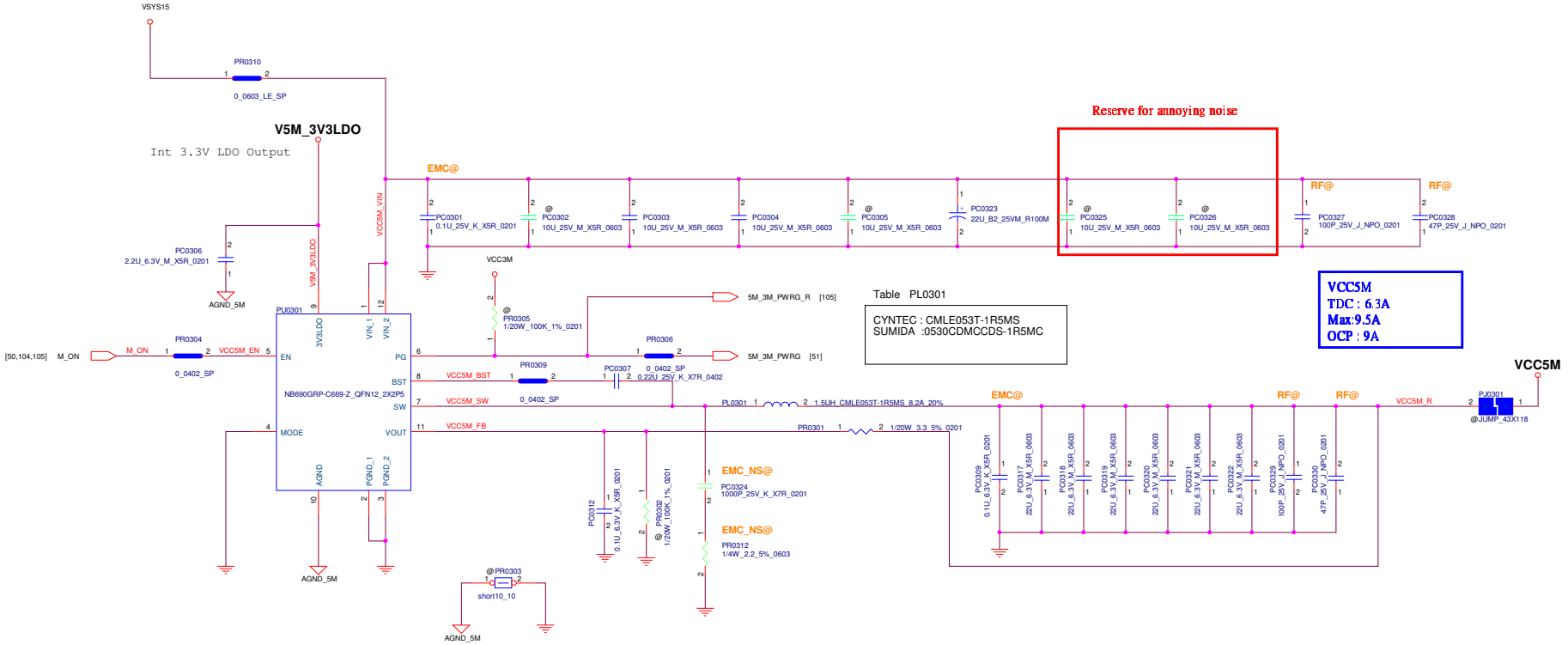

TABLE: NB690 Mode Control

RMode	MODE	VOUT	3V3LDO
0	Ceramic Cout	5.1V	3.3V
60K	POSCAP Cout	5.1V	3.3V
120K	Ceramic Cout	5V	3.3V
180K	POSCAP Cout	5V	3.3V
Floating	X	3.3V	3.3V

← LOGIC

Document Number	LCFC	
Size: Custom	Title: 103_DC/DC VCC5M (NB690)	Rev: 0.01
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TABLE1: NB693A CLM

Mode	CLM	Resister to GND
M1	7A	0
M2	10A	90K
M3	13A	150K
M4	16A	>230K or Float

LOGIC

TABLE 2: NB693A Mode 1 Control

Mode	VOUT	FS	Resister to GND
M1	Vo<3V, Vref=0.6V	700KHz	0
M2	Vo<3V, Vref=0.6V	1000KHz	90K
M3	Vo>=3V, Vref=1.8V	1000KHz	150K
M4	Vo>=3V, Vref=1.8V	700KHz	>230K or Float

LOGIC

VCC5_PD
TDC : 5.8A
OCP : 10A

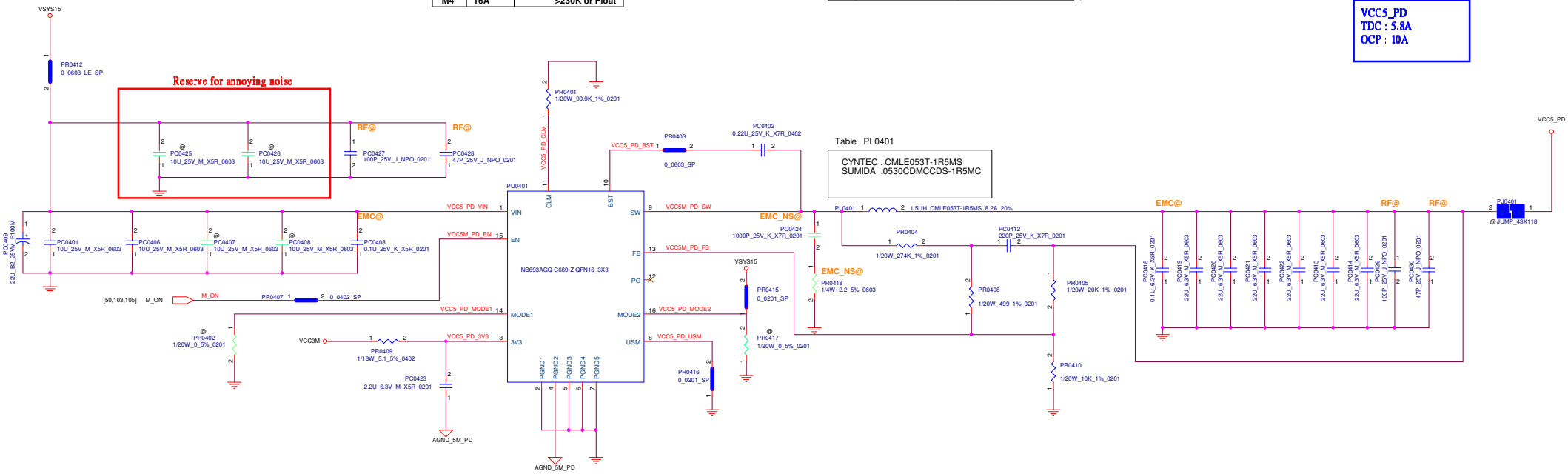

TABLE 3: NB693A MODE2 Selection

State	State	Mode2
M1	Internal Vcc	0
M2	External Vcc	Pull to VIN

LOGIC

TABLE 4: USM Selection

State	USM	Resister to GND
M1	Y	0
M2	N	Floating

LOGIC

@PR0411 short10_10 AGND_5M_PD

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Size: Custom	Title: 104_DC/DC VCC5_PD (NB693AGQ)		Rev: P1
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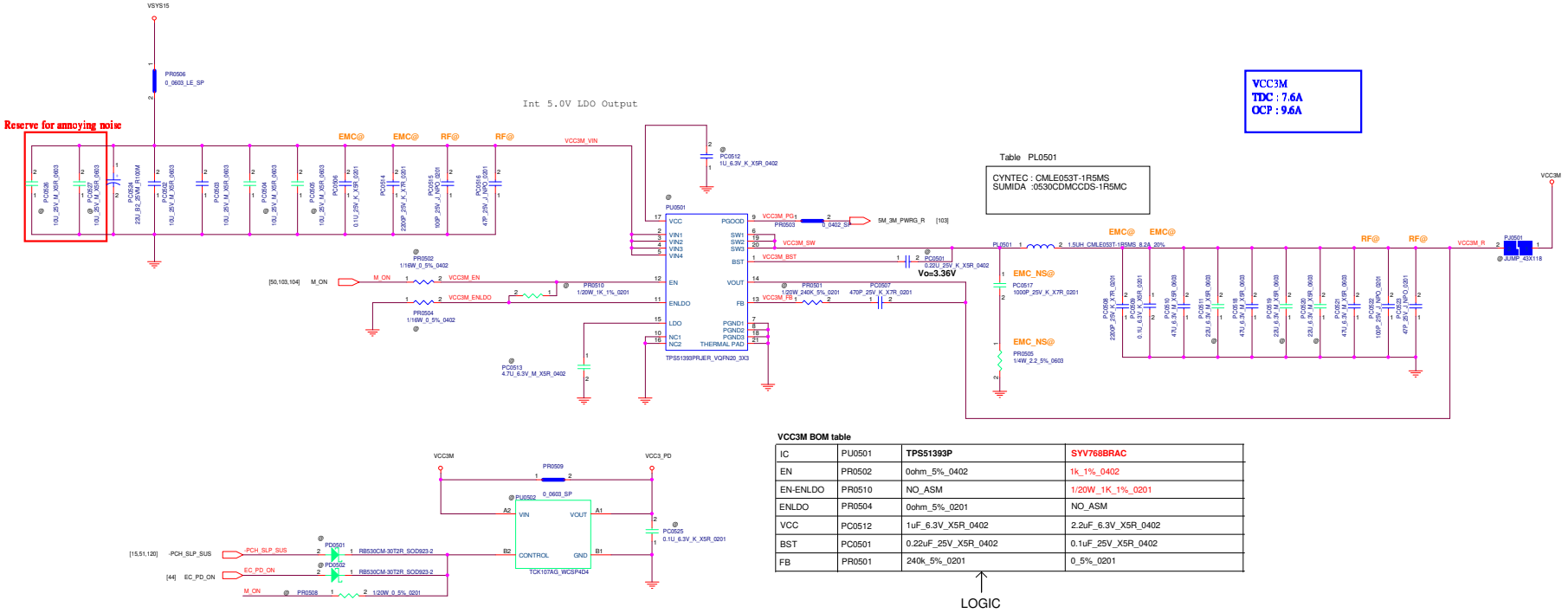

VCC3M BOM table

IC	PU0501	**TPS51393P**	**SYV768BRAC**
EN	PR0502	0ohm_5%_0402	1k_1%_0402
EN-ENLDO	PR0510	NO_ASM	1/20W_1K_1%_0201
ENLDO	PR0504	0ohm_5%_0201	NO_ASM
VCC	PC0512	1uF_6.3V_X5R_0402	2.2uF_6.3V_X5R_0402
BST	PC0501	0.22uF_25V_X5R_0402	0.1uF_25V_X5R_0402
FB	PR0501	240k_5%_0201	0_5%_0201

LOGIC

Document Number		LCFC	
Size: Custom	Title: *105_DC/DC VCC3M (TPS51393P)*		Rev: 0.01
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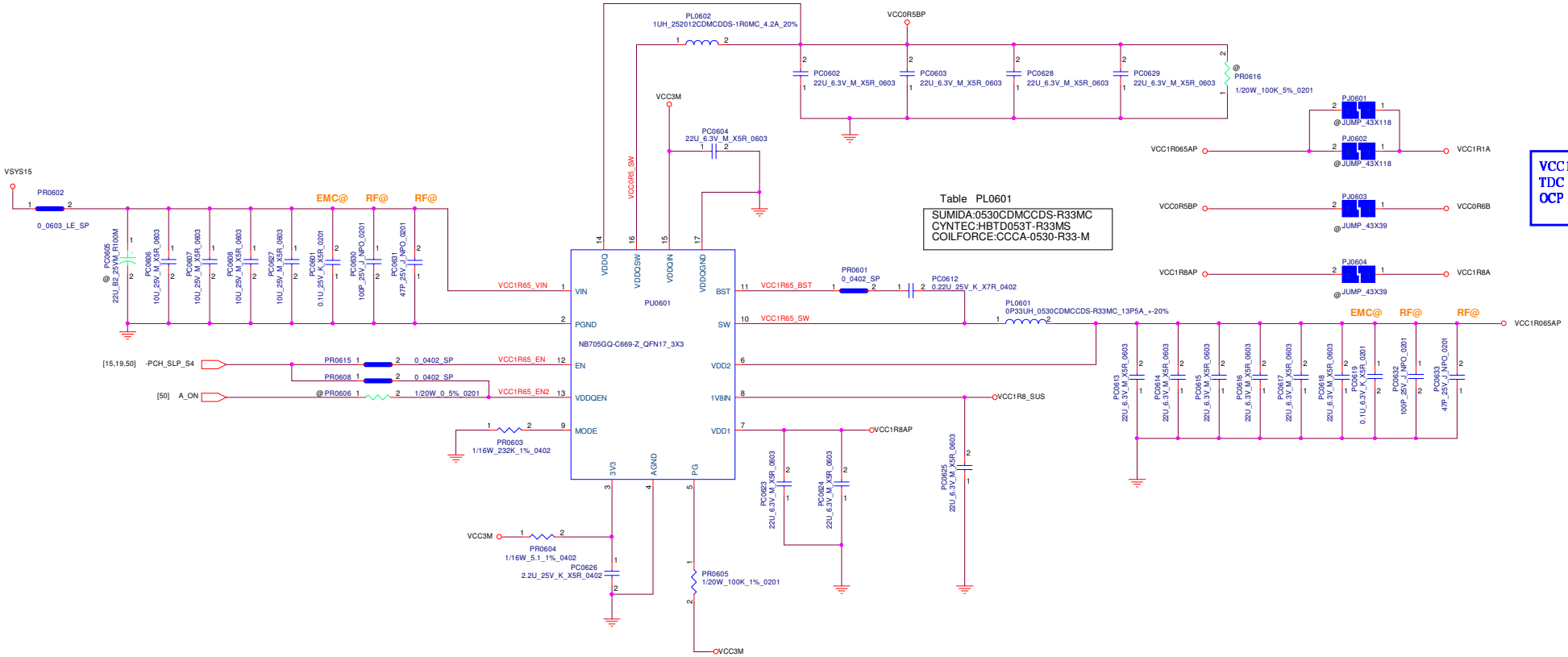
Table PL0602

SUMIDA: 252012CDMCDDS-1R0MC
CYNTEC: DFE252012F-1R0M=P2

Table PL0601

SUMIDA:0530CDMCCDS-R33MC
CYNTEC:HBTD053T-R33MS
COILFORCE:CCCA-0530-R33-M

VCC1R065A
TDC : 8A
OCP : 15A



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Document Number	LCFC	
Size: Custom	Title: 106_DC/DC VCC1R065A/(NB705)	Rev: 0.01
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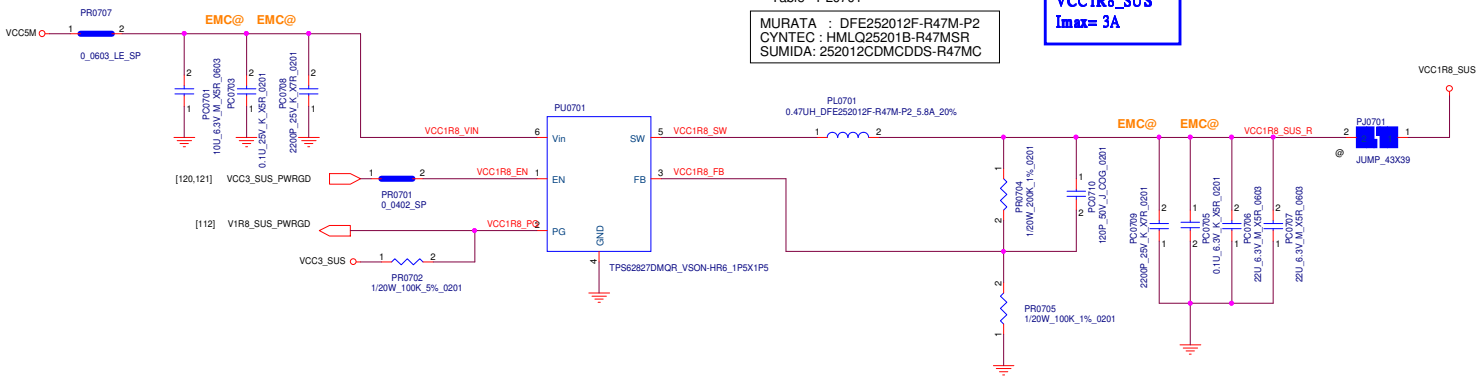
Table PL0701

MURATA : DFE252012F-R47M-P2
CYNTEC : HMLQ25201B-R47MSR
SUMIDA: 252012CDMCDDS-R47MC

VCC1R8_SUS
Imax= 3A



Document Number			LCFC
Size C	Title 107_DC/DC VCC1R8_SUS (TPS62827D		Rev 0.01
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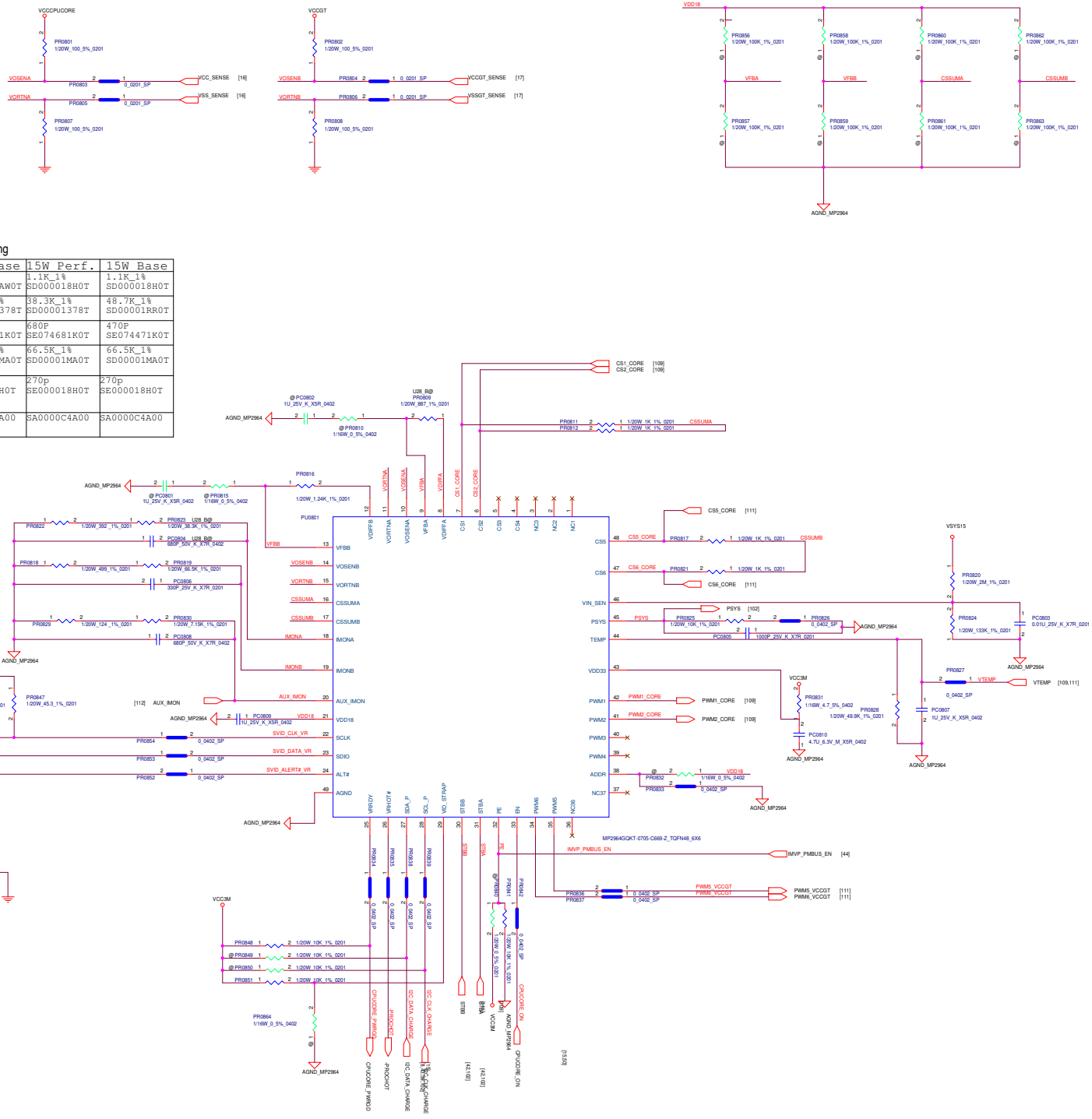
TABLE:MP2964 LL& IMON setting

		28W Perf.	28W Base	15W Perf.	15W Base
VCORE LL	PR0809	909_1% SD00001AW0T	909_1% SD00001AW0T	1.1K_1% SD000018H0T	1.1K_1% SD000018H0T
VCORE IMON	PR0823	29.4K_1% SD00002370T	38.3K_1% SD00001378T	38.3K_1% SD00001378T	48.7K_1% SD00001RR0T
	PC0804	680P SE074681K0T	680P SE074681K0T	680P SE074681K0T	470P SE074471K0T
VCCGT IMON	PR0819	56.2K_1% SD000013XPT	66.5K_1% SD00001MA0T	66.5K_1% SD00001MA0T	66.5K_1% SD00001MA0T
	PC0806	330p SE00000VG8T	270p SE000018H0T	270p SE000018H0T	270p SE000018H0T
IMVP9.1	PU0801	SA0000BSQ00	SA0000C4A00	SA0000C4A00	SA0000C4A00



Vcore: PWM1/2/3
28W Base TDC:47A IccMax:80A
15W perf TDC:43A IccMax:80A
15W base TDC:32A IccMax:60A

PC0937 Layput place near to Pin1

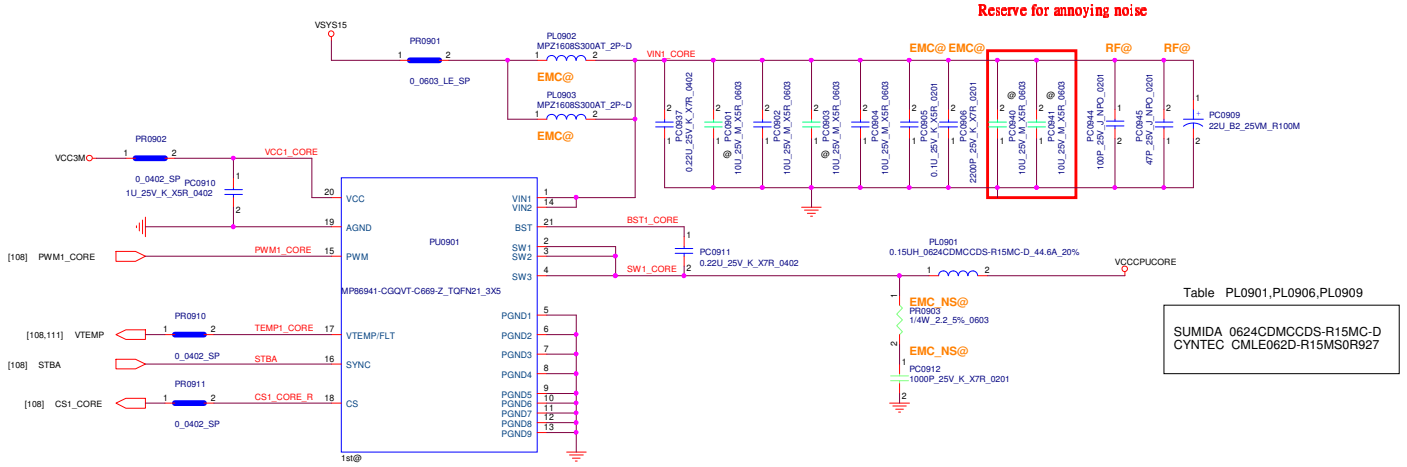
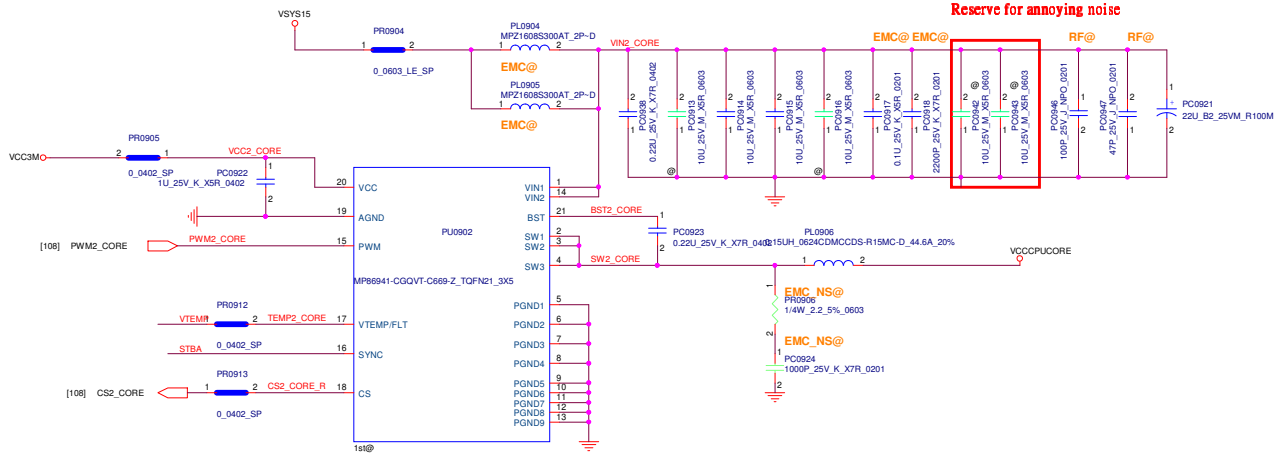


Table PL0901,PL0906,PL0909

SUMIDA 0624CDMCCDS-R15MC-D
CYNTEC CMLE062D-R15MS0R927

PC0938 Layput place near to Pin1



Document Number			LCFC
Size: Custom	Title: 109_DC/DC_VCCCPUCORE(MP86971		Rev: 0.01
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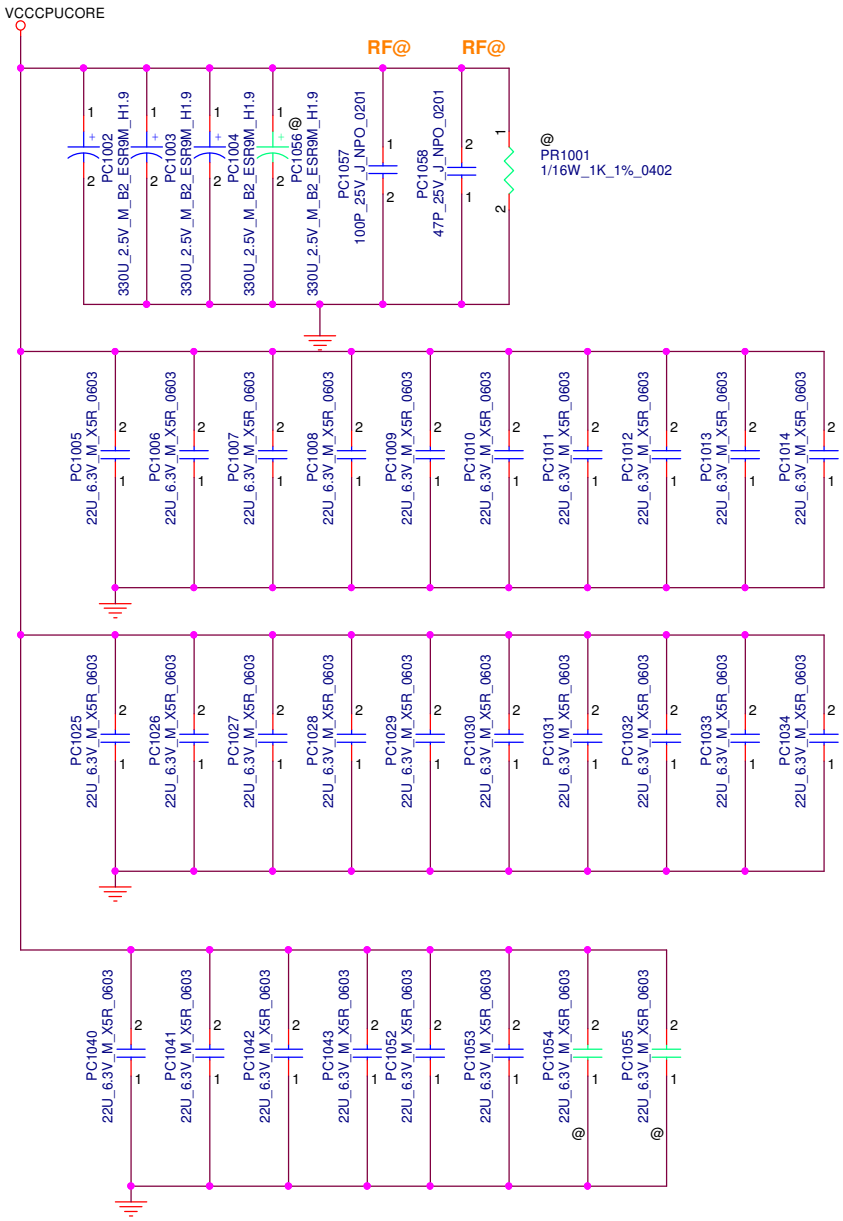

Document Number		LCFC
Size: Custom	Title: *110_DC/DC VCCCPUCORE_DE_CAP*	Rev: 0.01
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VccGT: PWM6/5
28W Base/15W performance/15W base TDC:23A IccMax:40A

VCCGT1-->PWM6/CS6
PC1168 Layput place near to Pin1

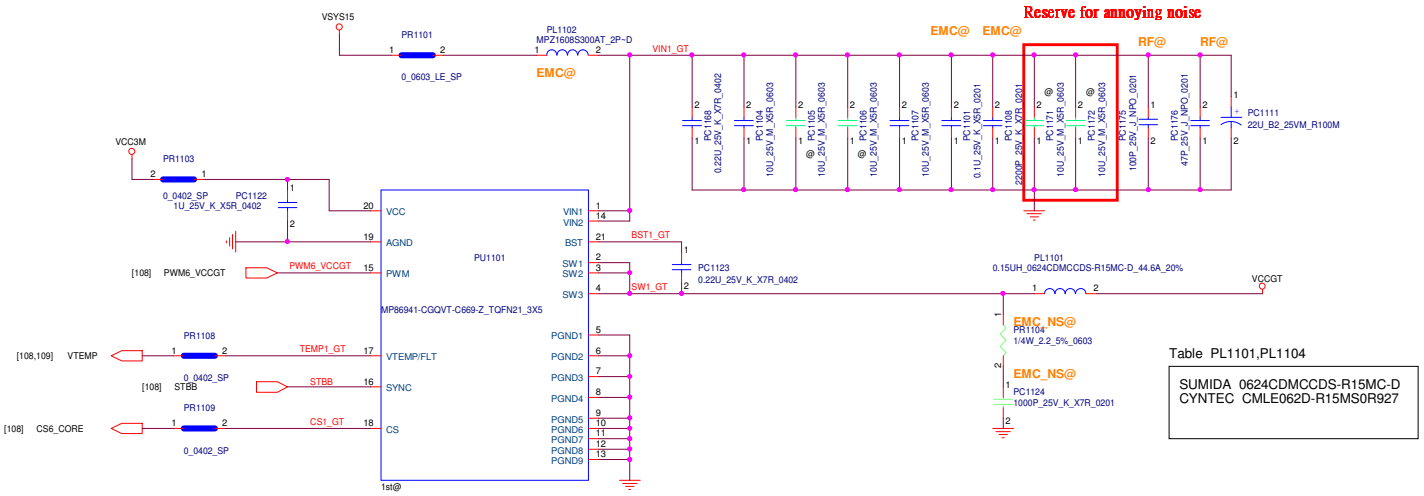
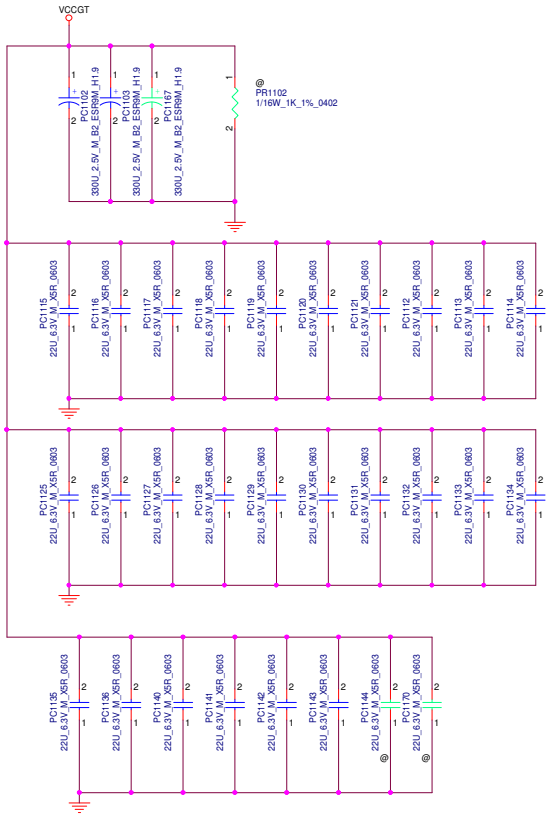
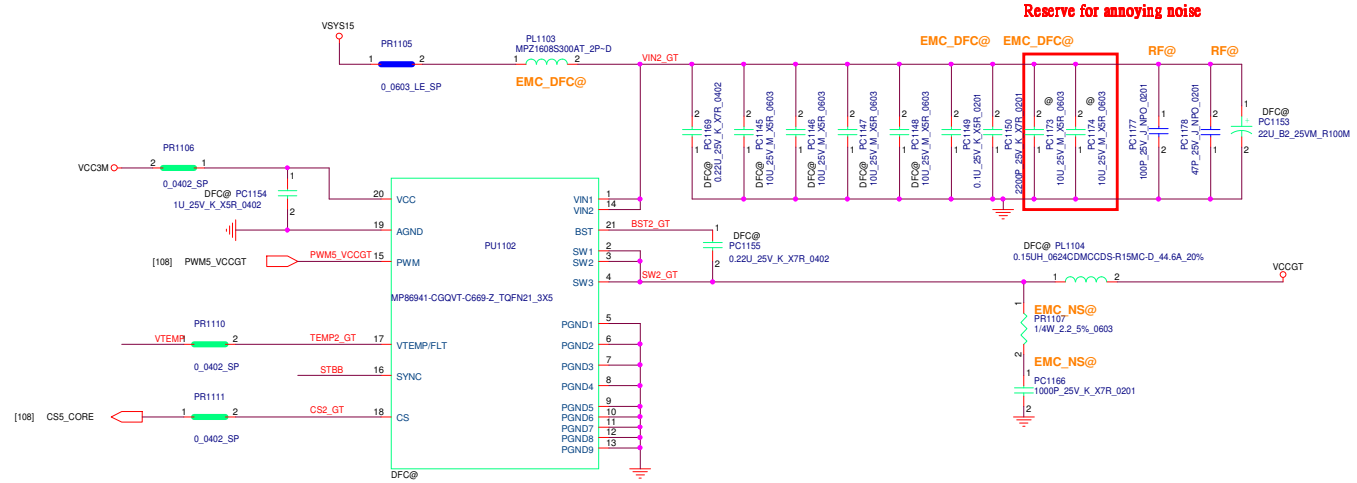


Table PL1101,PL1104

SUMIDA 0624CDMCCDS-R15MC-D CYNTEC CMLE062D-R15MS0R927



VCCGT2-->PWM5/CS5
PC1169 Layput place near to Pin1



Document Number		LCFC	
Size C	Title 111_DC/DC VCCGT(MP86943		Rev 0.01
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VccAUX:
TDC:14A IccMax:32A

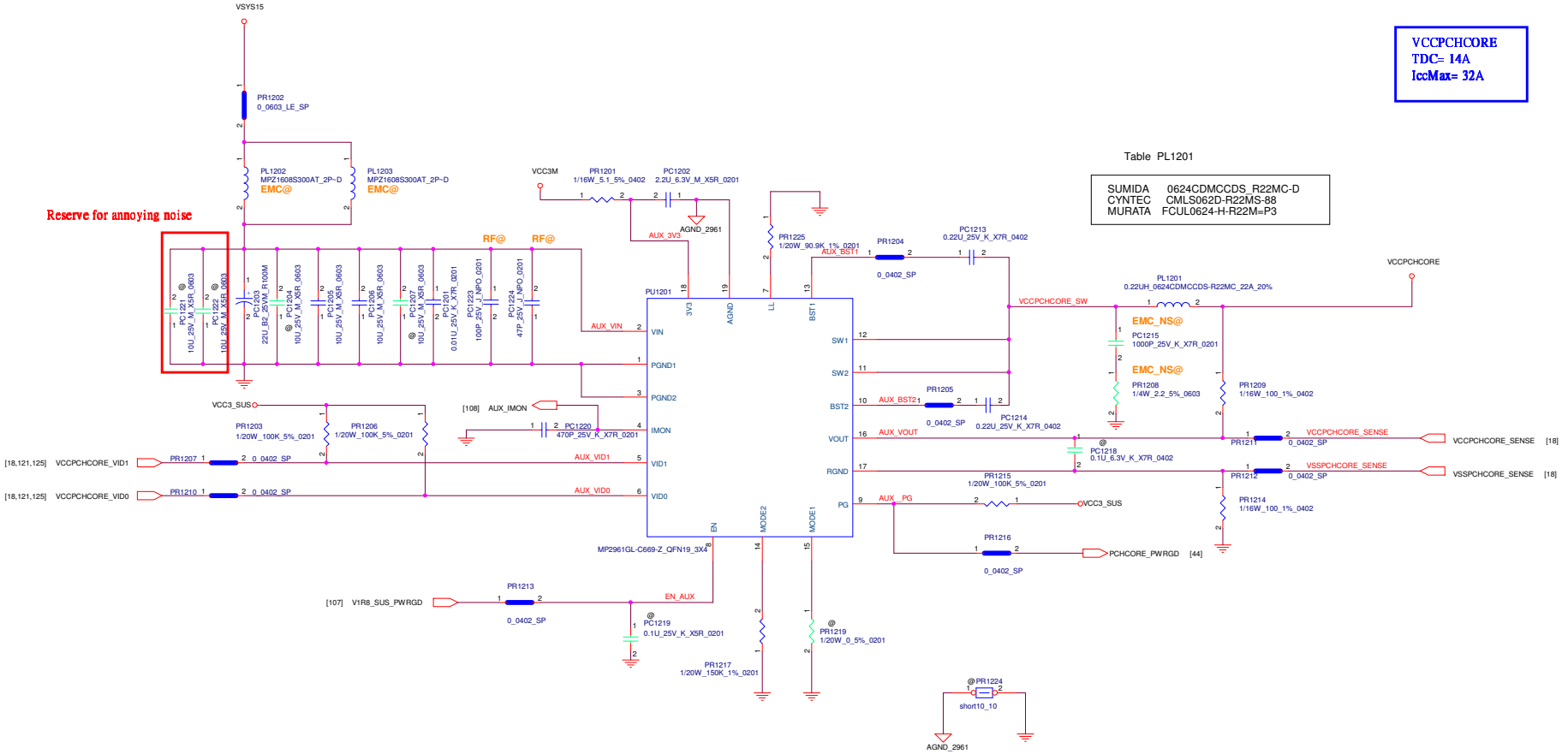


Table PL1201

SUMIDA	0624CDMCCDS_R22MC-D
CYNTEC	CMLS062D-R22MS-88
MURATA	FCUL0624-H-R22M=P3

Logic →

TABLE:MODE2 select

State	FS(KHz)	CLM	Resistor to GND
M1	800	12A	0
M2	1200	12A	90K
M3	800	17A	150K
M4	1200	17A	>230K or float

TABLE:LL

State	Load Line	Resistor to GND
M1	1m	0
M2	1.5m	90K
M3	2m	150K
M4	2.5m	>230K or float

← Logic

Logic →

TABLE:MODE1select

State	Interleaving	VID Down option	Resistor to GND
M1	No	Slew down	0
M2	Yes	Slew down	90K
M3	Yes	Decay	150K
M4	No	Decay	>230K or float

TABLE : VID control Bit logics

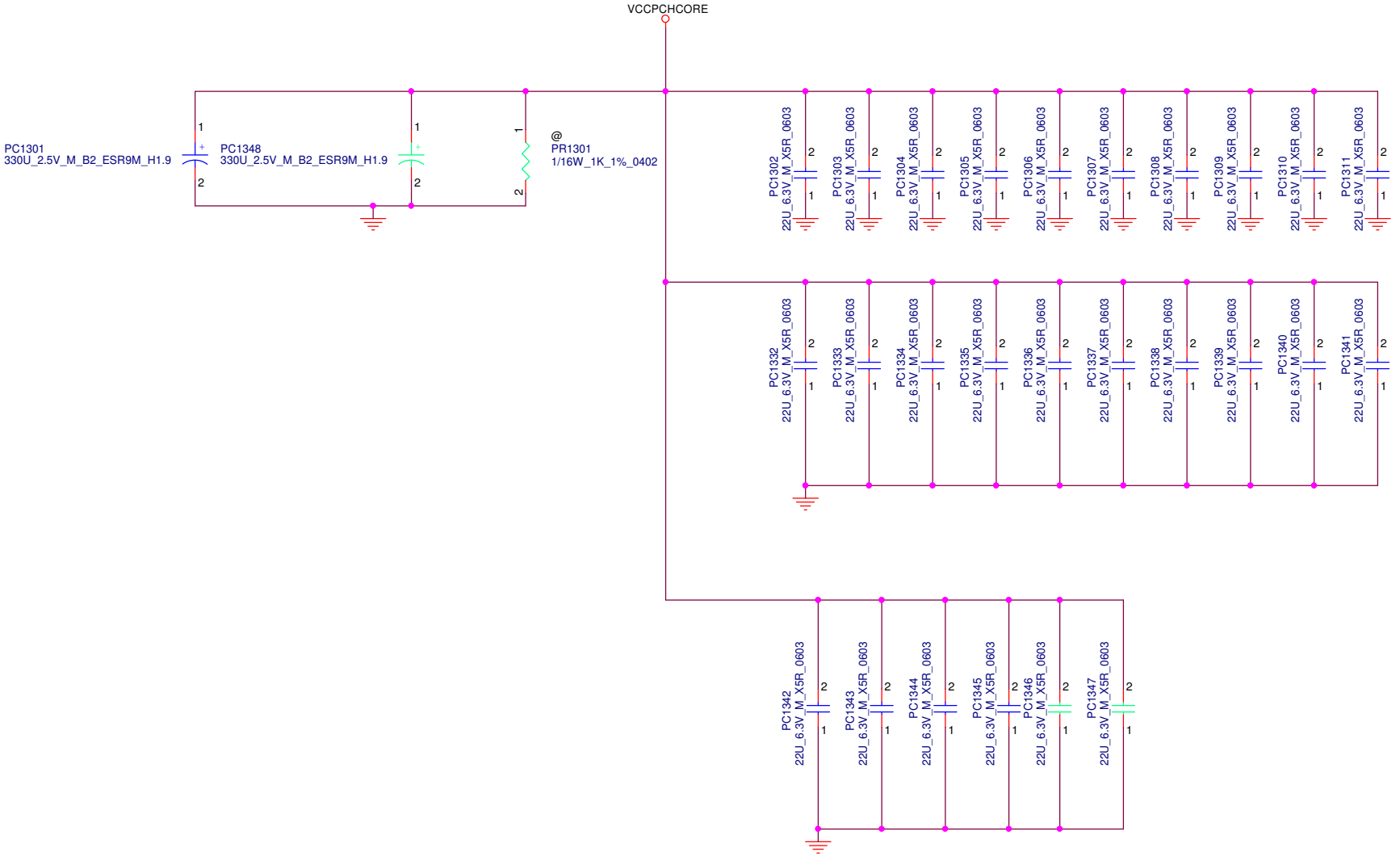
VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Document Number

LCFC

Size: Custom | Title: 112_DC/DC VCCPCHCORE(MP2961 | Rev: 0.01

Date: Tuesday, January 04, 2022 | Sheet 112 of 130



Document Number		LCFC
Size: Custom	Title: *113_DC/DC VCCPCHCORE DE_CAP*	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 113 of 130	

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Document Number		LCFC
Size: Custom	Title: *114_BLANK*	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 114 of 130	

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Document Number: DORAEMON			LCFC
Size: Custom	Title: BLANK		Rev: 0.01
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Document Number: DORAEMON		LCFC
Size: Custom	Title: BLANK	Rev: 0.01
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Document Number: DORAEMON			LCFC
Size: Custom	Title: BLANK		Rev: 0.01
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Document Number: DORAEMON		LCFC
Size: Custom	Title: BLANK	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 118 of 130	

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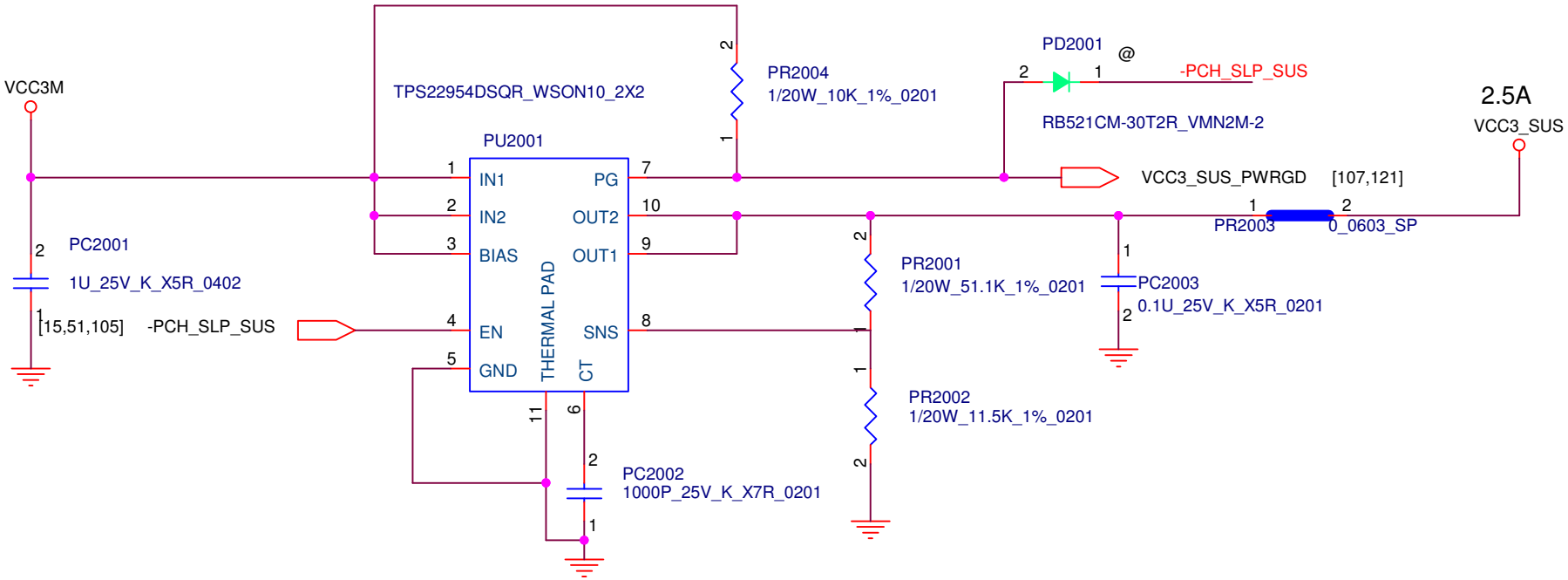
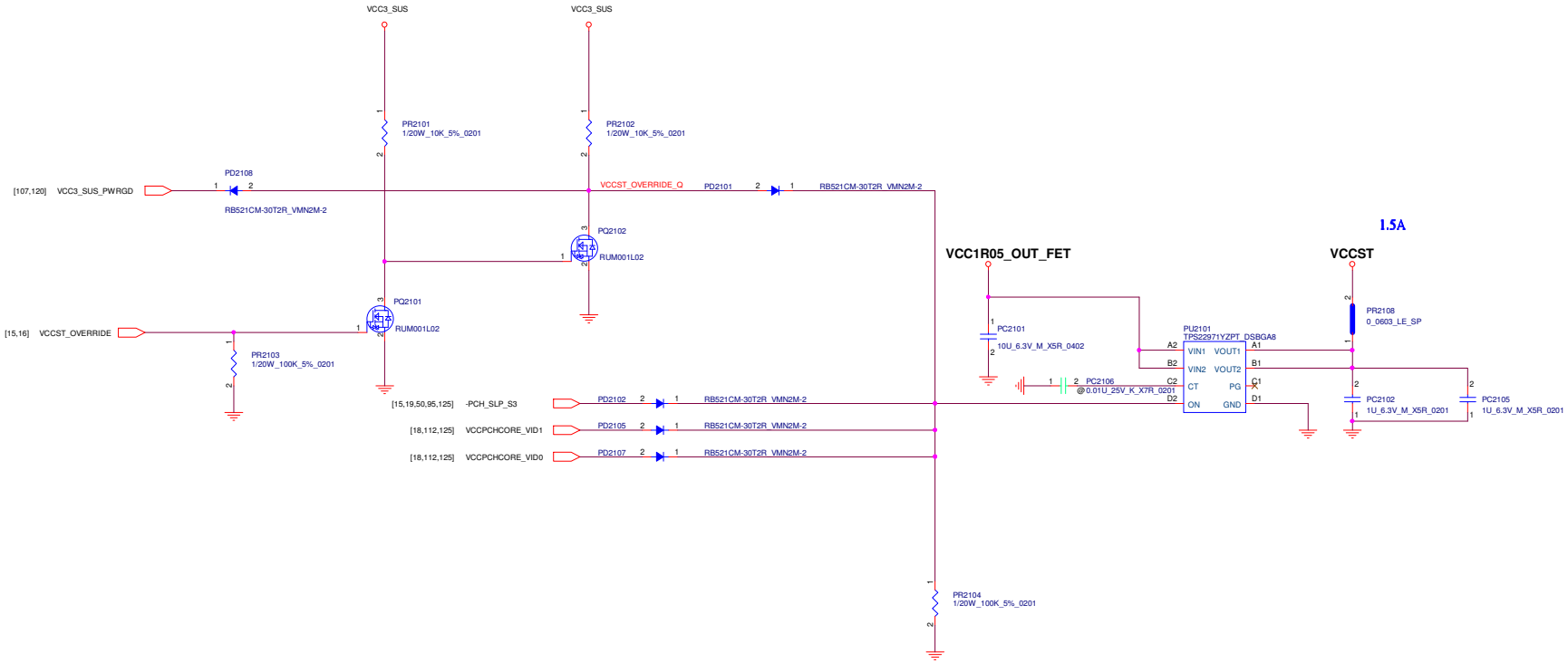
Document Number: DORAEMON		LCFC
Size: Custom	Title: BLANK	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 119 of 130	



Document Number	LCFC	
Size A	Title *120_LOAD SW VIDEO*	Rev 0.01
Date: Tuesday, January 04, 2022	Sheet 120 of 130	



Document Number			LCFC
Size: Custom	Title: 121_LOAD SW VCCST & VCCSTG		Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 121 of 130		

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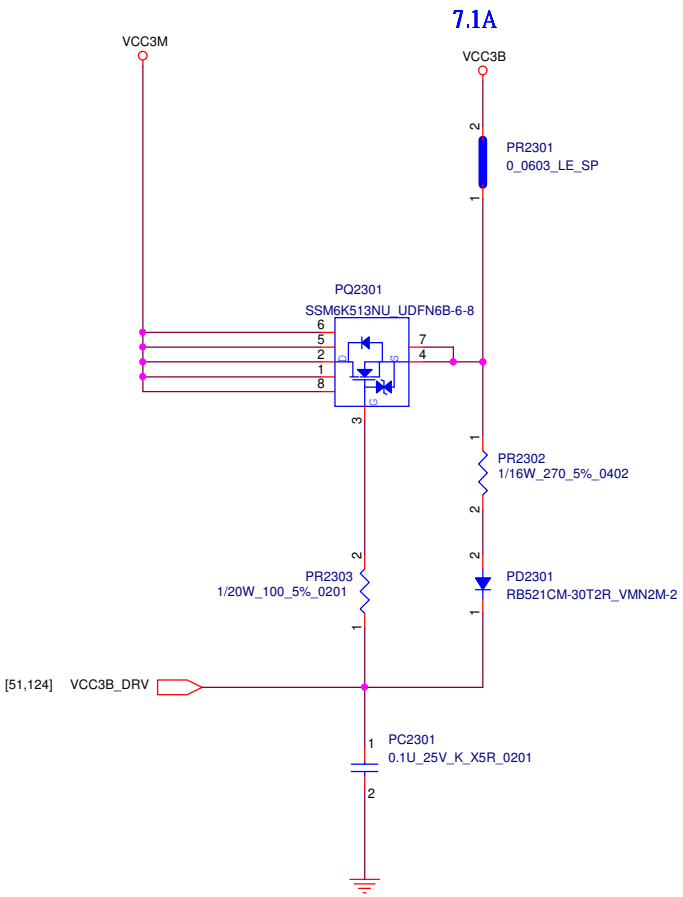
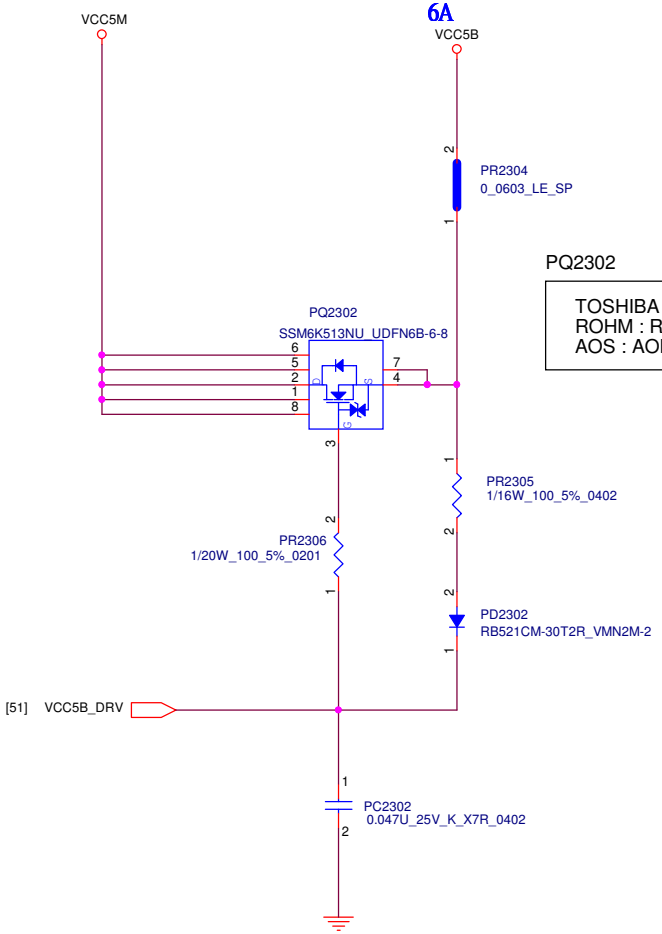
Document Number	LCFC	
Size: Custom	Title: *122_BLANK*	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 122 of 130	



PQ2301

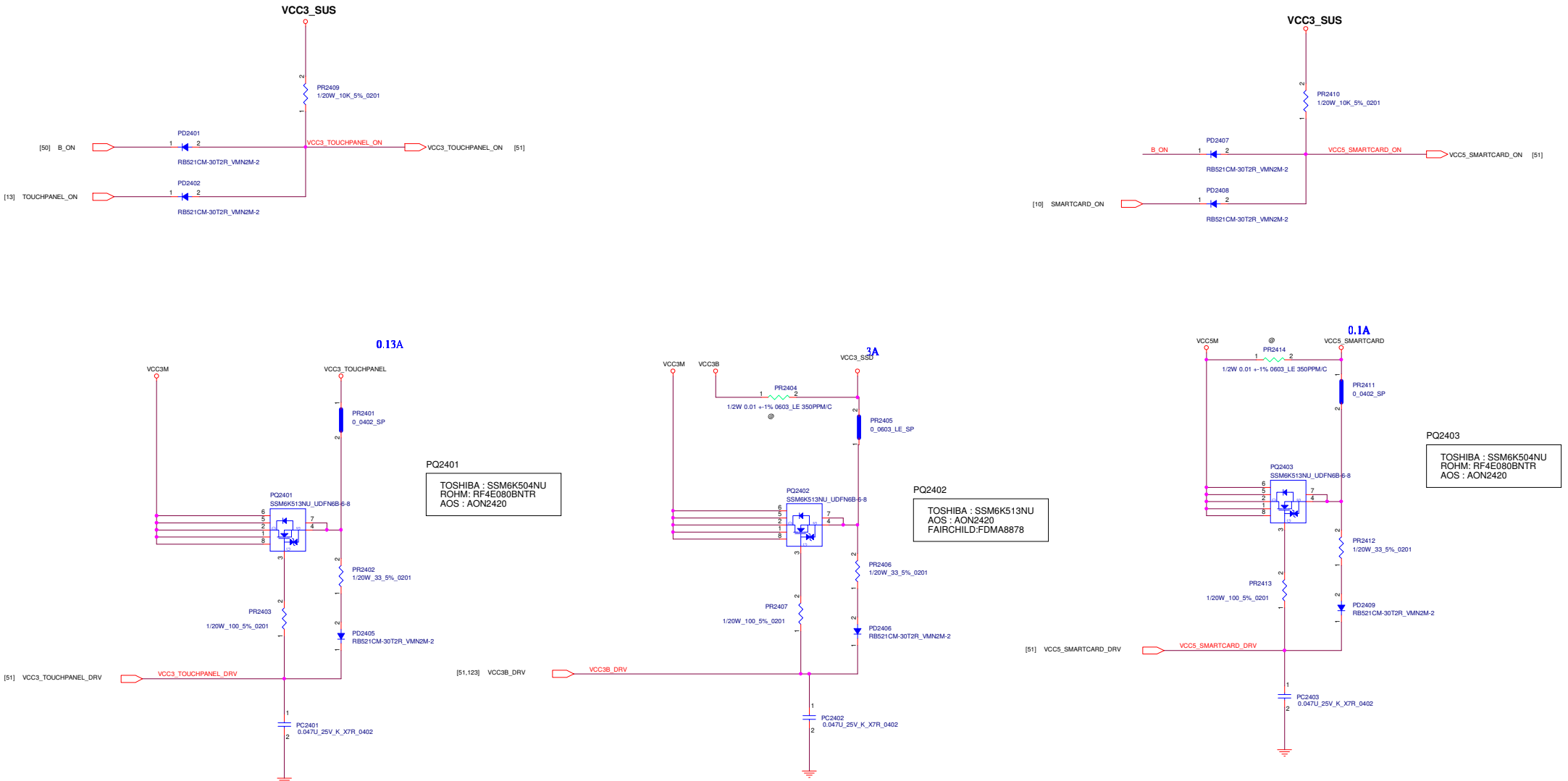
TOSHIBA : SSM6K513NU
AOS : AON2420
FAIRCHILD : FDMA8878



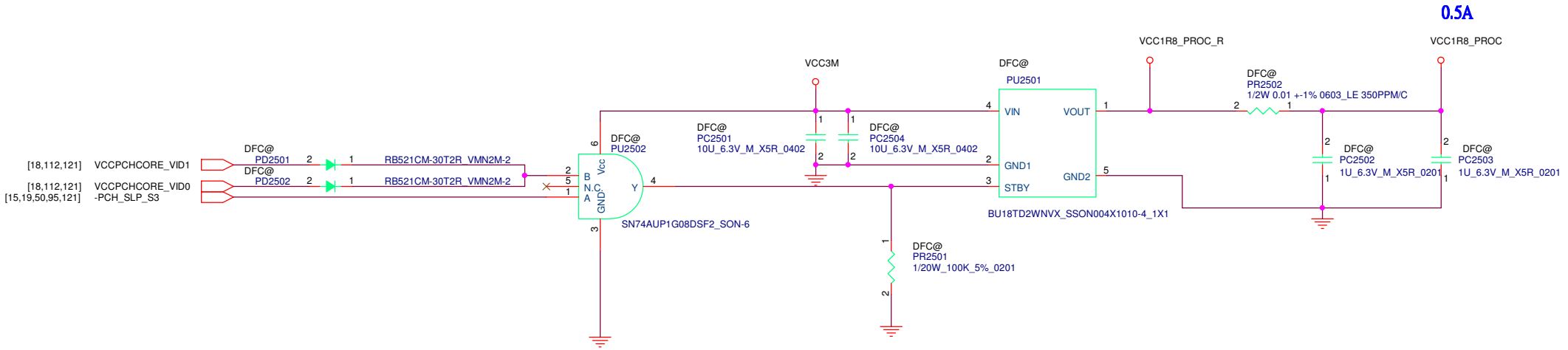
PQ2302

TOSHIBA : SSM6K504NU
ROHM : RF4E080BNTR
AOS : AON2420

Document Number		LCFC
Size: Custom	Title: 123_LOAD SW B	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 123 of 130	



Document Number		LCFC
Size: Custom	Title: 124_LOAD SW TOUCH PANEL	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 124 of 130	



Document Number	LCFC	
Size: Custom	Title: *125_VCC1R8_PROC*	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 125 of 130	

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Document Number			LCFC
Size: Custom	Title: *126_BLANK*		Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 126 of 130		

PR0809
U15_P@
1/20W 1.1K +-1% 0201

PR0823
U15_P@
1/20W 38.3K +-1% 0201

PC0804
U15_P@
680P_50V_K_X7R_0402

PR0809
U15_B@
1/20W 1.1K +-1% 0201

PR0823
U15_B@
1/20W 48.7K +-1% 0201

PC0804
U15_B@
470P_50V_K_X7R_0402

PU0901
2nd@
MP86941GQVT-C669-Z

PU0902
2nd@
MP86941GQVT-C669-Z

PU1101
2nd@
MP86941GQVT-C669-Z

X76_E
X76_E
X764E90100E
X76_E@

X76_F
X76_F
X764E90100F
X76_F@

X76_G
X76_G
X764E90100G
X76_G@

Charger BOM table

IC	PU0201	BQ25710RSNR	SC8885LQDER
ACP	PR0202	4.99ohm_1%_0201	10ohm_1%_0201
ACN	PR0203	4.99ohm_1%_0201	10ohm_1%_0201
ACP	PC0214	0.033uF_10%_25V_0402	NO_ASM
ACN	PC0215	0.033uF_10%_25V_0402	NO_ASM
COMP1	PR0205	40.2k_1%_0201	100k_1%_0201
COMP1	PC0223	1800pF_10%_25V_0201	1000pF_10%_25V_0201
COMP1	PC0224	33pF_5%_25V_0201	10pF_5%_25V_0201
COMP2	PR0206	10k_1%_0201	330k_1%_0201
COMP2	PC0225	680pF_10%_25V_0201	1000pF_10%_25V_0201
COMP2	PC0226	15pF_5%_25V_0201	220pF_10%_25V_0201
ILIM_HIZ	PR0210	174k_1%_0201	137k_1%_0201
CELL_BATPRESZ	PR0209	33.2k_1%_0201	16.5k_1%_0201

X76

Charger
BQ25710RSNR_QFN32_4X4
X764E90100C
BQ25710_X76@

PU0201
BQ25710RSNR_QFN32_4X4
SA00009K300
BQ25710@

PR0202
1/20W_4.99_1%_0201
SD000018D0T
BQ25710@

PR0203
1/20W_4.99_1%_0201
SD000018D0T
BQ25710@

PC0214
0.033U_25V_K_X7R_0402
SE00000YI0T
BQ25710@

PC0215
0.033U_25V_K_X7R_0402
SE00000YI0T
BQ25710@

PR0205
1/20W_40.2K_1%_0201
SD000013G8T
BQ25710@

PC0223
1800P_25V_K_X7R_0201
SE00000ZY0T
BQ25710@

PC0224
33P_25V_J_NPO_0201
SE174330JMT
BQ25710@

PR0206
1/20W_10K_1%_0201
SD041100ZYT
BQ25710@

PC0225
680P_25V_K_X7R_0201
SE00000WYMT
BQ25710@

PC0226
15P_25V_J_NPO_0201
SE00001ZJ0T
BQ25710@

PR0210
1/20W_174K_1%_0201
SD00002270T
BQ25710@

PR0209
1/20W_33.2K_1%_0201
SD00011A8T
BQ25710@

Charger
SC8885LQDER
X764E90100D
SC8885_X76@

PU0201
SC8885LQDER
SA0000CTY00
SC8885@

PR0202
1/20W_10_1%_0201
SD041100APT
SC8885@

PR0203
1/20W_10_1%_0201
SD041100APT
SC8885@

PC2509
0.033U_25V_K_X7R_0402
SE00000YI0T
@

PC2510
0.033U_25V_K_X7R_0402
SE00000YI0T
@

PR0205
1/20W_100K_1%_0201
SD04110030T
SC8885@

PC0223
1000P_25V_K_X7R_0201
SE170102KMT
SC8885@

PC0224
10P_25V_J_NPO_0201
SE000011G0T
SC8885@

PR0206
1/20W_330K_1%_0201
SD00001ZD0T
SC8885@

PC0225
1000P_25V_K_X7R_0201
SE170102KMT
SC8885@

PC0226
220P_25V_K_X7R_0201
SE00000RGMT
SC8885@

PR0210
1/20W_137K_1%_0201
SD00002210T
SC8885@

PR0209
1/20W_16.5K_1%_0201
SD00001XV0T
SC8885@

VCC3M
TPS51393PRJER_VQFN20_3X3
X764E90100A
TPS51393_X76@

PU0501
TPS51393PRJER_VQFN20_3X3
SA00009A200
TPS51393@

PR0502
1/16W_0_5%_0402
SD0280000YT
TPS51393@

PR0510
1/20W_1K_1%_0201
SD0411001PT
@

PR0504
1/16W_0_5%_0402
SD0280000YT
TPS51393@

PC0512
1U_6.3V_K_X5R_0402
SE000000KMT
TPS51393@

PC0501
0.22U_25V_K_X5R_0402
SE00001780T
TPS51393@

PR0501
1/20W_240K_5%_0201
SD00002D40T
TPS51393@

VCC3M
SYV768BRAC_QFN_20P
X764E90100B
SYV768_X76@

PU0501
SYV768BRAC_QFN_20P
SA0000CHC00
SYV768@

PR0502
1/16W_1K_1%_0402
SD03410018T
SYV768@

PR0510
1/20W_1K_1%_0201
SD0411001PT
SYV768@

PR0504
1/16W_0_5%_0402
SD0280000YT
@

PC0512
2.2U_6.3V_K_X5R_0402_YAGEO
SE00000W1YT
SYV768@

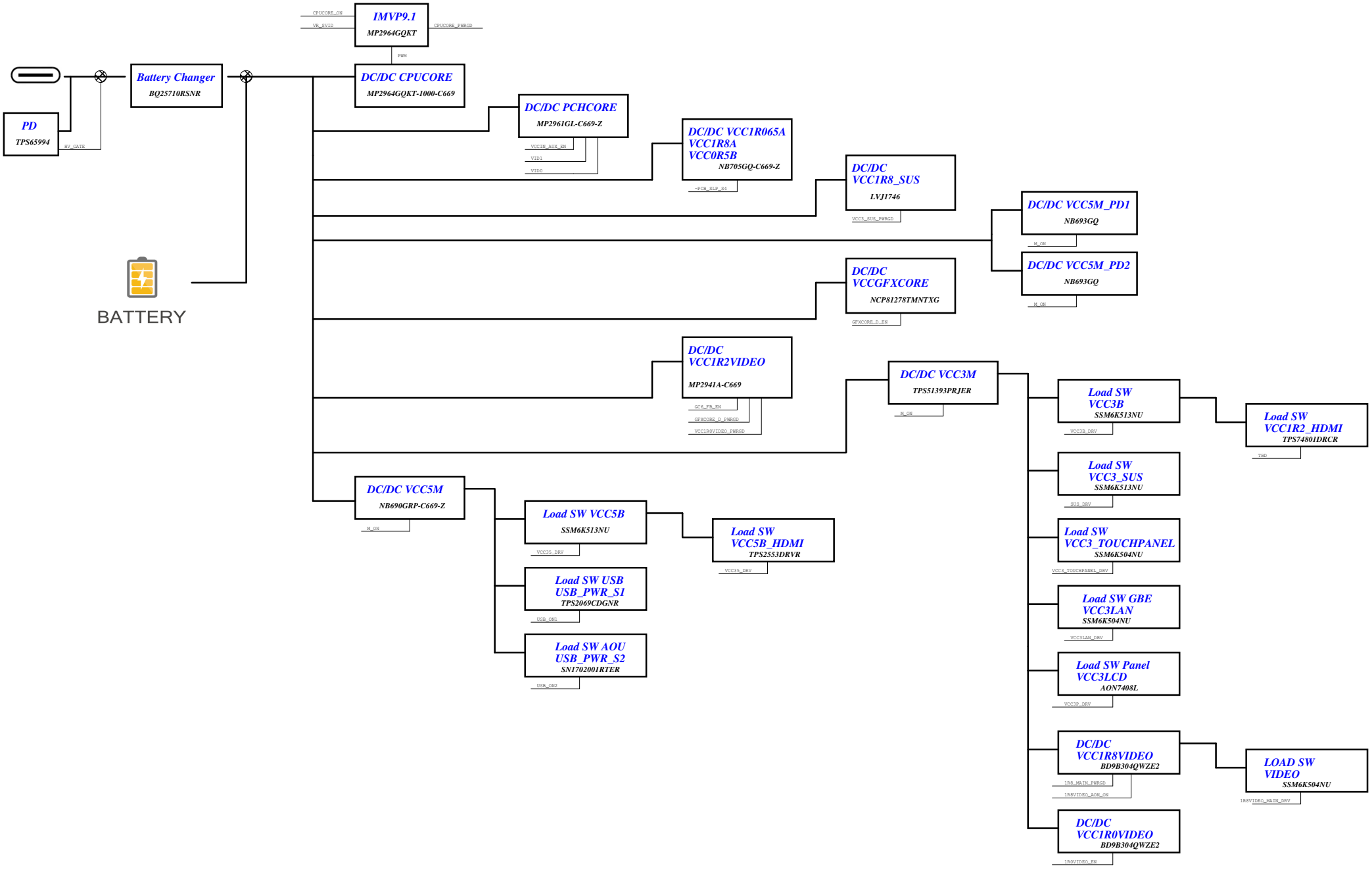
PC0501
0.1U_25V_K_X5R_0402
SE00000G80T
SYV768@

PR0501
1/20W_0_5%_0201
SD0430000YT
SYV768@

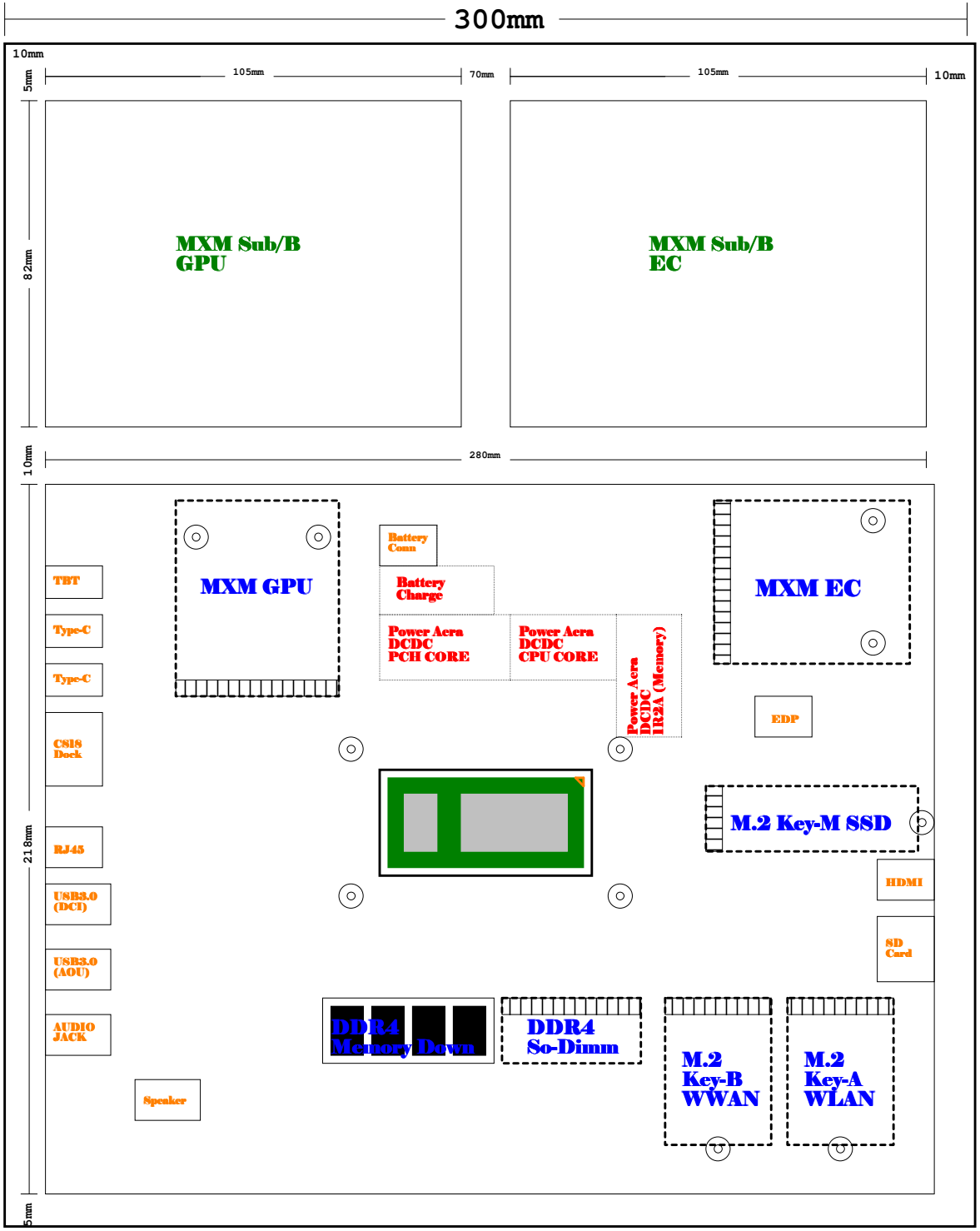
VCC3M BOM table

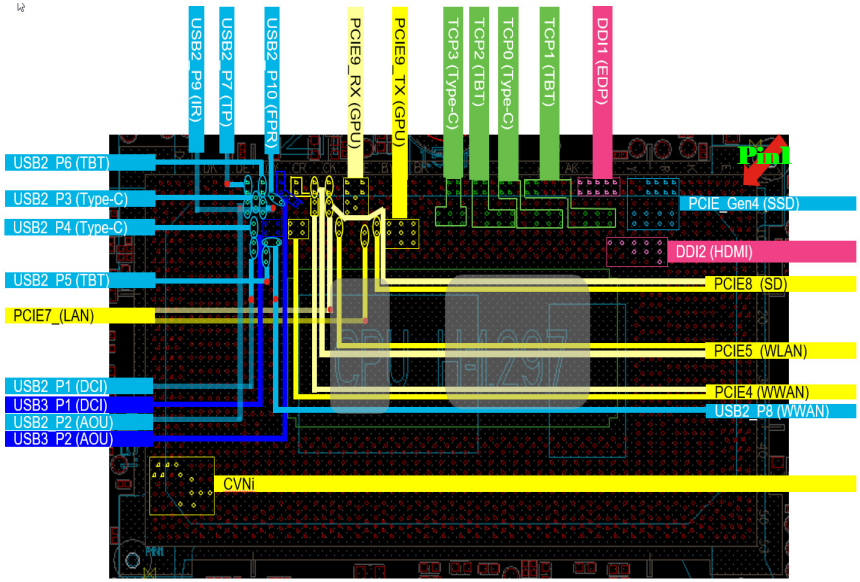
IC	PU0501	TPS51393P	SYV768BRAC
EN	PR0502	0ohm_5%_0402	1k_1%_0402
EN-ENLDO	PR0510	NO_ASM	1/20W_1K_1%_0201
ENLDO	PR0504	0ohm_5%_0201	NO_ASM
VCC	PC0512	1uF_6.3V_X5R_0402	2.2uF_6.3V_X5R_0402
BST	PC0501	0.22uF_25V_X5R_0402	0.1uF_25V_X5R_0402
FB	PR0501	240k_5%_0201	0_5%_0201

Document Number
LCFC
Size Custom
Title 127_BLANK
Rev 0.01
Date: Monday, January 10, 2022
Sheet 127 of 130



Document Number			LCFC
Size: Custom	Title: 128_System Power Tree		Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 128 of 130		





Document Number: DORAEMON		LCFC
Size: Custom	Title: 129_Plancement	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 129 of 130	

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Document Number: DORAEMON			LCFC
Size: Custom	Title: 130_BLANK		Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 130 of 130		